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Mapping China's semiconductor ecosystem in global context

Strategic Dimensions
and Conclusions



MERICS

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Executive Summary

Historically, the semiconductor value chain has flourished thanks to transnational divisions of labor that supported high levels of economic efficiency and innovation. As a result, interdependencies throughout this value chain exist between different regions around the globe. The US-China technology rivalry, the COVID19 pandemic and global shortages in semiconductors have led many governments to scrutinize these interdependencies in the transnational semiconductor value chain. The US government for example has completed a review of the semiconductor supply chain. Europe's new industrial strategy focuses on assessing and managing strategic dependencies in different technology ecosystems, including semiconductors.

China's capabilities in the semiconductor value chain play a key role in these considerations. China's government is making great efforts to raise the competitiveness of Chinese industry in the semiconductor sector, building on and supporting China's role in global electronics manufacturing and emerging technological ecosystems. With growing strategic concerns in the US and Europe about China, a better understanding and systematic assessment of China's capabilities in producing semiconductors is needed. What is the position within the semiconductor value chain of Chinese companies? In which areas is China highly reliant on foreign technology providers? How likely is China to catch up within this decade in a particular production step?

This report provides a framework for assessing the national interest vis-à-vis China's role in the semiconductor value chain. We draw conclusions across three strategic dimensions – industry competitiveness, national security and resilience of the global supply chain – that impact the interests of all nations, given the importance of semiconductors in the modern world. Understanding China's role throughout the value chain in terms of these strategic dimensions helps policy makers to identify current and future interdependencies with China, and to balance or prioritize between competing interests. With this picture, European decisionmakers are better equipped to best position EU countries for a world in which technological interdependence is increasingly contested, weaponized and fraught with national risk.

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Introduction

Semiconductors are the foundation of almost every application of electronics. Often combined in an “integrated circuit” (IC) and commonly called “chips,” semiconductors are a strategic technology on which national power is increasingly dependent. Yet their value chain is among the most globalized of any industry.

This value chain is extensive, complex and built on a transnational division of labor, due to economic pressure to innovate and thus, to specialize. This division of labor has created a host of cross-border interdependencies, with different global regions specializing in different production steps. A particular semiconductor often is designed in the United States (US), manufactured in Taiwan using chemicals from Japan and Germany and equipment from the Netherlands, and assembled and packaged in China. Within this complex value chain, many process steps and inputs are indispensable but are often under the control of only a few companies. In some cases, a particular input can be effectively monopolized by a single company.

The transnational nature of the value chain conflicts with the national interest perspective now increasingly brought to the semiconductor sector by governments, politicians and policy commentators. What exactly “strategic importance” means in the context of the semiconductor value chain is often not well articulated. However, these policy debates recognize the critical role of the value chain’s end products in a range of applications, and the potential for the value chain’s interdependencies to be ‘weaponized’ by one nation against another.¹ These national interest factors are driving efforts to reduce dependency on foreign providers by strengthening the domestic semiconductor ecosystem—the complex of enterprises, research institutions, skilled labor, investment capital and other factors that underpin research and development (R&D) and production.

Given growing political concerns in Western countries about China, China’s position in the semiconductor value chain and in the applications built on top of chips is seen as a potential threat that must be mitigated. But the cost of mitigation measures based on cutting China out of the global value chain is potentially large, and the success of such efforts uncertain.² It is also unclear whether European nations would benefit from such decoupling to the same degree as the US and other players in the semiconductor value chain. The starting point for such discussions should be a comprehensive understanding of China’s semiconductor ecosystem, its role in the global value chain and the implications from a national interest perspective, with as much specificity as possible.

This report provides an overview of China's position in the semiconductor value chain by analyzing its position in the different production steps and providing an analytical framework for drawing conclusions about the strategic implications. In section 1, we explain our general approach focusing on the value chain's distinct production steps, and for each step, on China's domestic ecosystem in the global context. For each step, we offer conclusions from a national interest perspective, organized by three strategic dimensions that capture the differing implications of these interests.

In section 2, we provide an overview of China's semiconductor ecosystem in general, focusing on the most recent phase of state-led policy for the semiconductor sector. In section 3, we analyze the eight distinct production steps in the value chain separately, following the template described in section 1. Glossaries for technical terms and for Chinese institutions and documents (including acronyms) are provided in annexes 1 and 2, respectively, at the end of the report. A list of selected Chinese documents concerning the semiconductor sector is provided in Annex 3.

In section 4, we draw summary conclusions about China's role in the global value chain as a whole, focusing on important takeaways for European policymakers. A second report published in late 2021 will look further into these conclusions in the international context and offer policy recommendations from a European perspective.



1. Analytical approach

Focus on the value chain

Because the global semiconductor value chain is fragmented functionally and geographically, it should be understood within the context of distinct production steps. We identify eight production steps: They consist of three process steps (design, fabrication, and assembly, test and packaging) and five inputs in the process steps (software, intellectual property (IP), equipment, chemicals and wafers; see Fig. 1).

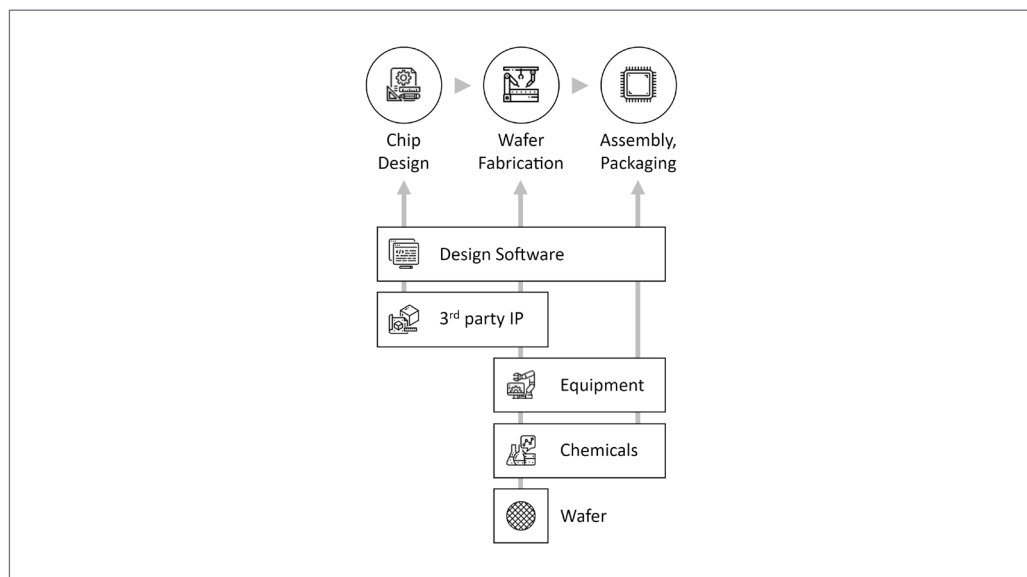


Fig. 1:
Production steps
(process steps
and inputs) in the
semiconductor
value chain

Focusing on these generic production steps allows us to analyze the competitiveness of China's domestic semiconductor value chain, its dependence on foreign technology providers and the likelihood of China's increased self-reliance and international competitiveness in the future. In section 3, we look at all eight production steps separately, China's position within them and the implications from a national interest perspective, according to the following template:

- **Overview:** What is the general function of the production step, and how does it relate to the rest of the value chain?
- **Market structure:** What is the current market situation? Who are the dominant players? Are there monopolies or oligopolies?
- **Barriers to entry:** How hard would it be for a new company to enter this market profitably?
- **The Chinese government's effort to increase self-reliance:** To what extent has the production step received policy attention from the Chinese government? How effective has this been?



- **Competitive position of the Chinese industry:** What is the competitive position of Chinese companies in this production step?
- **Likelihood of China catching up within 5 to 10 years:** How likely is it that China's industry will catch up with the global market leaders in the coming decade?
- **Strategic dimensions:** How do these elements affect national interests, in general terms and in relation to China's position in this specific production step?

Assessment of strategic dimensions for each production step

After mapping each production step based on the template above, we offer a short assessment of the strategic importance of the step. We structure this assessment in terms of three **strategic dimensions**. Each dimension corresponds to three criteria for assessing strategic importance, which distill insights from the mapping. These dimensions and criteria represent different aspects of national interest. Together, they explain why in the context of a particular production step governments are motivated to take measures that promote their own industry and that of allies or constrain the capabilities available to adversaries.

Strategic dimensions and criteria

The **competitiveness dimension** captures commercial and technical implications of the production step's market landscape, which affect the economic and technological bases of national power, in the context of a competitive international environment. Criteria include the following:

- **Revenue capture:** The financial returns that accrue with dominant market share. Financial returns vary between production steps, with some significantly more lucrative than others.
- **Barriers to entry:** The difficulty of a new player establishing itself in this production step. High barriers to entry are significant when dominant market share is held by a few actors, because they make efforts to replicate these capabilities costly and uncertain of success.
- **Spillover benefits:** The potential for capabilities in this production step to stimulate activity elsewhere in the value chain, or in other industry sectors.

The **national security dimension** involves a production step's significance for zero-sum competition between nation-states. These implications reflect the potential for 'weaponization' by national governments to actively damage the interests of other nations. Criteria include the following:

- **Espionage risk:** The potential for manipulation of a given production step to facilitate intelligence gathering against or sabotage of the interests of rival nations.



For example, assembly, test and packaging (ATP) present relatively significant opportunities for espionage activity.

- **Military utility:** The significance to national military capabilities. For example, chip design capabilities are more important than those in ATP for the capacity of a national economy (or an alliance of economies) to build sophisticated military platforms, such as fighter aircraft.
- **Chokepoint:** The potential for dominant market share in a production step to be weaponized against nations lacking these capabilities, for example, through national and multilateral export controls that target specific nations.

The **resilience dimension** addresses the semiconductor value chain as a whole, that is, on a global scale. As the value chain is globally integrated, disruptions have negative impacts on national interests generically, regardless of adversarial relations between particular nations. Every nation suffers from a resilience failure that disrupts the international value chain as a whole. Criteria include the following:

- **Concentrated point of failure:** These failure points represent business continuity risks to the global value chain as a whole from natural disasters, pandemics or political interventions. Such points are a product of decades of technical specialization and transnational division of labor.
- **Spillover damage:** This represents the potential for the disruption of a given production step to flow to other segments of the global value chain, and to other industrial sectors. An example can be seen in the current problems facing the automobile manufacturing industry worldwide, stemming from constraints in wafer fabrication.
- **Replicability:** The implications of attempting to replicate a given production step, through government intervention, in nations where it is not currently concentrated. Replicating production in this way can increase the global value chain's resilience through national and geographic diversification. However, such efforts also risk wasting resources and hampering innovation, by changing the economies of scale and transnational division of labor that have given the semiconductor value chain its current form.

Distinguishing between these strategic dimensions allows us to understand why a national government would try to strengthen its own semiconductor ecosystem, including in cooperation with allies, or to undermine that of its adversaries. For example, even if there are few economic reasons (such as low revenue capture, high barriers to entry) to invest in domestic capabilities for a particular production step, if it constitutes a chokepoint for domestic industry due to reliance on foreign technology providers, a nation might try to strengthen its own industry in that production step.



These strategic dimensions in each production step are not specific to China: Barriers to entry, espionage risk, spillover damage and the other criteria all have the same implications from the perspectives of all nations. Thus, our **matrix** (see Fig. 2) provides a generic overview or heat map of the semiconductor value chain across the strategic dimensions we describe in the mapping. The color codes show to what extent one of the criteria applies to a specific production step. For example, the **barriers to entry** (for any company, in any nation) for a given production step can be low, moderate, substantial or high.

The matrix provides the basis for assessments in the **strategic dimensions** section in each production step chapter. In these sections, we explain the strategic importance of each production step, listed by the criteria we described above. We also provide conclusions specifically about China's current position in each production step and the country's likely progress over the next decade. We evaluate China's behavior and include evaluations of responses by other nations.

For example, the military utility of end products based on chip design capabilities is a substantial reason for the Chinese government to promote chip design capabilities domestically, but from a U.S. viewpoint, this is a substantial reason to restrict such development in China. These imperatives are compounded by the progress China has made in this production step, as well as China's potential to support further progress with demand for semiconductors generated by other sectors of the Chinese economy.

This approach helps the reader to compare national interests and risks that differ in type and operate in different contexts, which potentially implies conflicting choices in response. What to prioritize, and how to resolve trade-offs, are for the reader to decide. In the conclusion in section 4, we highlight what we consider the most important issues from a European viewpoint.

The following examples illustrate how to read this matrix, in conjunction with the strategic dimensions analysis for each production step:

- **Design:** Given **high revenue capture**, **high spillover benefits** and **low barriers to entry**, China will likely continue to substantially support its domestic chip design ecosystem. China also has substantial incentives in terms of potential benefits for supporting the development of chips that have **military utility**, representing a source of risk for nations that view China as a potential adversary.
- **SME:** Despite a relatively **low revenue capture** and **substantial barriers to entry**, China will try to decrease its reliance on foreign semiconductor manufacturing equipment (SME) vendors because SME provides the US and its allies with a **substantial chokepoint** to exploit against China. If China succeeds in establishing competitive domestic SME vendors, there will be **substantial spillover benefits**, because SME is a critical input for wafer fabrication.



- **ATP**: Assembly, test and packaging (ATP) has relatively **low revenue capture** and currently, only **moderate spillover benefits**. As the importance of advanced packaging is increasing, these aspects will certainly change in the future. The **high espionage risk** associated with this production step is of little concern to China, as it holds a substantial share of the packaging market. Thus, it is highly likely that China will try to upgrade its packaging ecosystem to ensure a strong market position in the future.

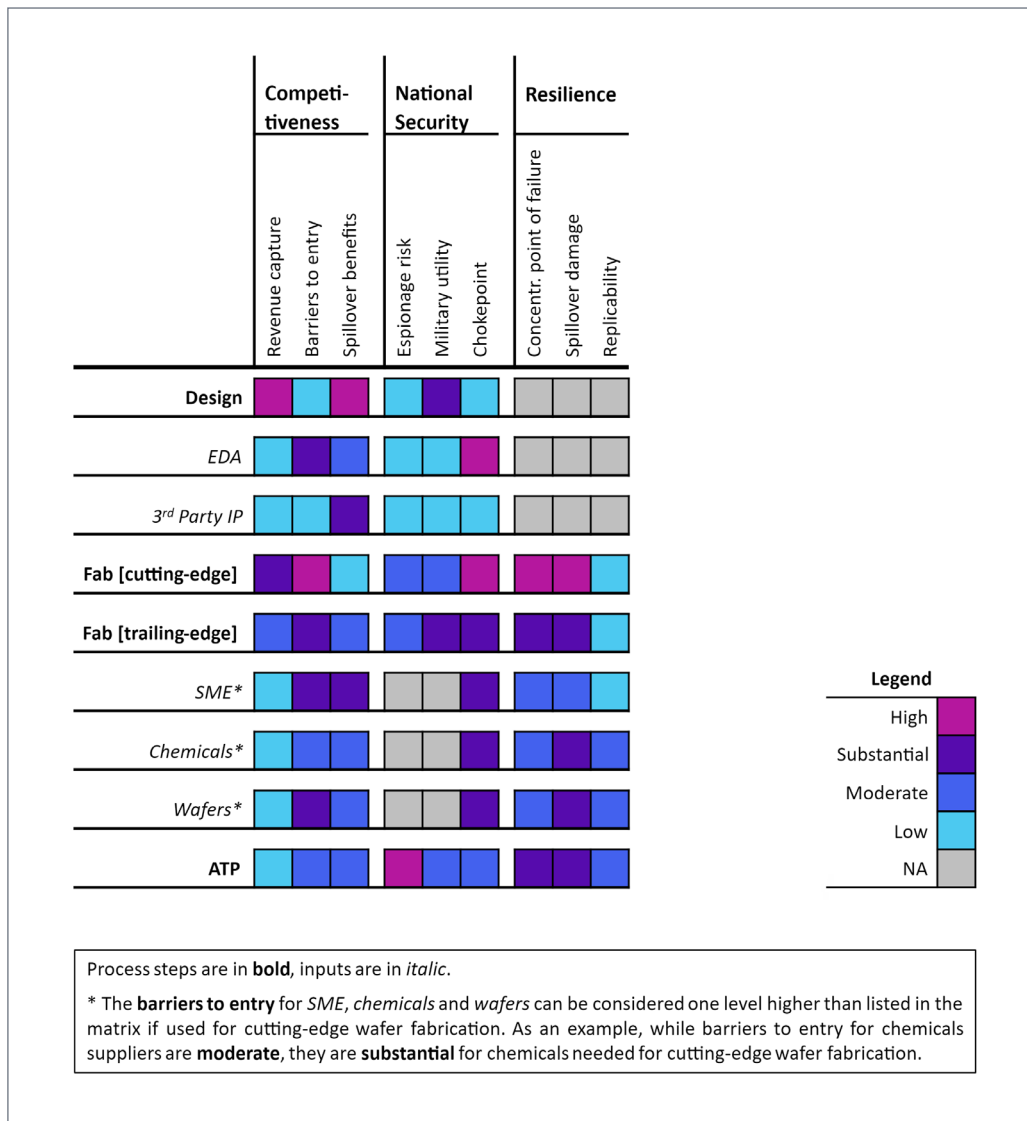


Fig. 2: Strategic dimensions per production step (overview)



2. China's semiconductor ecosystem

Larger national policy context

China's policy for the semiconductor sector sits within a larger framework **for science and technology development**, which is articulated in various directive policy statements issued by China's central government authorities. Key principles underlying this framework include the following:

- The assessment that information technology (IT) and digitalization have become foundational to national economies and therefore, to national power, in a competitive international environment;
- The continued centrality of the physical ("real") economy and manufacturing, and the need to deeply integrate the real economy with IT to achieve broad-based technological leadership;
- Recognition that China is still lagging global leaders in core technologies, a source of national vulnerability that must be mitigated by increasing China's relative capabilities;
- Recognition that closing the gap in technological capabilities requires maintaining a degree of international openness in China's economy and connections to foreign technological leaders.

China's policy for the semiconductor industry over the past decade

Semiconductors have been targeted by official Chinese policies for several decades, although progress in closing the gap with foreign industry leaders across the value chain remains limited.³ In the following paragraphs, we describe the important aspects of the most recent phase of Chinese official policy for the semiconductor sector. These aspects are captured by a **schematic** representing how Chinese state-led policy operates across the entire sector (Fig. 3).

China's senior leaders seem to have understood Chinese industry's critical foreign dependencies since at least 2009, when national agencies instituted the **02 Special Project**. This aimed to "break China's dependence on imports" across various segments of the semiconductor value chain, by assigning R&D projects to enterprises and research institutions.⁴ A 2017 progress report identified some successes⁵: For example, it claimed that Chinese suppliers had commercialized 16 types of front-end wafer fabrication equipment; one product was approved by global foundry leader *TSMC* for an advanced (7 nanometer, 'nm') process node.⁶



The 2014 National IC Industry Development Outline

In 2014, the State Council, China's highest executive government agency, issued the *National Integrated Circuit Industry Development Outline* (the 2014 Outline). This is often identified as starting the current phase of China's semiconductor policy, marked by less direct state intervention than in the past and by extensive state-led funding across the board rather than favoring of a few selected firms.⁷

The 2014 Outline sought to improve centralized policy coordination by creating a national steering committee (**Leading Small Group, LSG**), supported by an advisory expert committee. The IC Industry LSG's director is a Vice-Premier of the State Council and member of the Chinese Communist Party's (CCP) Politburo, Ma Kai, and its deputy director (often the key executive role in such bodies) is the head of the Ministry of Industry and Information Technology (MIIT), Miao Wei. Both men hold corresponding positions in a separate LSG for "building China into a manufacturing superpower," reflecting the connections between semiconductors and the wider electronics and manufacturing sectors.⁸

It is unclear to what extent the national IC LSG remains active or involved in policymaking. In June 2021, media reporting suggested that the impetus behind national-level policymaking for the semiconductor industry was shifting to the LSG for 'reform of the national science and technology system and building an innovation system' (**ST&I LSG**).⁹ This body is headed by Liu He, chief economic adviser to Chinese President Xi Jinping, and China's lead negotiator for trade talks with the U.S. government during the Trump administration. The precise relationship between these two LSGs is unclear. The same is true for the extent of coordination with 'leading small groups' for semiconductor policy created by several subnational governments in the last few years (Annex 2).

The 2014 Outline listed development targets for chip design, fabrication, packaging and test, manufacturing equipment and materials.¹⁰ It aimed to promote upgrades in all these segments of the value chain through direct financing and tax relief measures, and through state-linked equity investment funds at the national and regional levels.¹¹ Accordingly, the 2014 Outline established the National Integrated Circuit Industry Investment Fund (Big Fund), incorporated in late 2014 with registered capital of RMB 98.72 billion (more than USD 15 billion).

State-linked investment funds

The **Big Fund** represents a type of state-led industrial policy instrument now common in China across foundational and emerging technology sectors: the so-called

'government guidance fund.' Such funds use the limited partnership structure typical of equity finance worldwide, but they are set up by state agencies that provide anchor capital and influence investment decisions. State involvement aims to attract investment from other sources such as China's private sector and foreign investors, although in practice a dominant role is often played by state-owned enterprises and other state-linked actors.¹² These state-linked investment funds may also be a means of avoiding World Trade Organization (WTO) restrictions on direct subsidies: the Big Fund was named in a U.S. complaint at the WTO in 2018.¹³

The Big Fund is overseen by the MIIT and the Ministry of Finance.¹⁴ Most shareholders are state-owned enterprises and other government guidance funds; the bulk of the capital raised during **Phase I** came from the Ministry of Finance and the state-owned China Development Bank (CDB).¹⁵ The Big Fund's managing entity (Sino-IC Capital) has been run in succession by two executives from CDB, which also owns 45% of Sino-IC.¹⁶

Subnational IC investment guidance funds were also established during 2014 in existing centers of China's semiconductor industry.¹⁷ The Shanghai government-linked fund was established in partnership with a private investment fund, a common model for government guidance funds that seeks to leverage private sector expertise.¹⁸ As of mid-2020, 14 province-level governments had set up their own investment funds for the IC sector, totaling around RMB 300 billion (USD 45 billion).¹⁹

Phase I of the Big Fund closed in 2019, having raised RMB 138.7 billion (more than USD 20 billion).²⁰ Around two thirds of the fund's investments went to fabrication and the other manufacturing-related categories of SME and materials, while approximately 20% were made in the chip design sector and around 10% in assembly, test and packaging.²¹ At the close of Phase I, Sino-IC Capital declared that the total capital expenditure in China's semiconductor sector had doubled over 2014–2017, compared to the preceding four years.²² Chinese state media reported that Phase I attracted five times the sum of capital it raised (that is, around RMB 500 billion) to China's semiconductor sector from other financing sources.²³

Phase II of the Big Fund was incorporated in October 2019 with registered capital of RMB 204.15 billion (more than USD 32 billion). The shareholder mix expanded to include entities representing a wider geographical spread of China's semiconductor sector, which may improve the overall quality of the investments.²⁴ The state hopes that Phase II achieves the same 1:5 investment multiplier ratio that was claimed for Phase I.²⁵ This would result in an additional **RMB 1 trillion (more than USD 150 billion)** of investment in China's semiconductor sector. However, this amount of funding does not appear to be guaranteed by Chinese authorities, although it is sometimes portrayed this way in international media reporting.



The Big Fund's Phase I prioritized investments in fabrication, as directed in the 2014 Outline. Chinese state media reporting when Phase II was incorporated indicated that future investments would focus more on SME and on applications downstream in the value chain, thus dragging along development of upstream sectors. Cited as precedent for such an outcome is the previous upgrading of China's mobile device supply chain that was driven by Apple's manufacturing operations in China.²⁶

Other supporting policies for the semiconductor sector

In 2015, the State Council issued the **Made in China 2025** (MiC 2025) industrial upgrading plan, which set widely reported targets of attaining 40% self-sufficiency in China's total IC consumption by 2020, and 70% by 2025. An accompanying **roadmap** prepared by the Chinese Academy of Engineering listed more specific targets for technology development, including for the semiconductor sector.²⁷ In 2017, a national 'IC Industry Technical Innovation Strategic Alliance' was established to coordinate among research and industry actors with the aim of "making China's IC industry technology innovation capabilities reach internationally leading levels in 5-10 years".²⁸

In response to U.S. export controls that have targeted multiple Chinese firms by exploiting the Chinese industry's foreign dependencies in electronic design automation (EDA) and SME (including indirectly, through dependence on non-mainland firms such as *TSMC*), since mid-2020 Chinese national agencies have introduced three sets of measures providing **targeted support** that include tax relief, direct financing and subsidies, regulatory guidance and skills development.²⁹ These measures build on similar policy packages issued by national authorities over the last decade, notably in 2011.³⁰

Subnational governments are also taking measures to provide sustained support to Chinese firms operating in the semiconductor sector. For example, in March 2021, the Lingang Special Area in Shanghai's designated free trade zone released a five-year plan to develop the IC industry, including a bonded R&D and manufacturing zone where materials and inputs can be imported duty-free.³¹

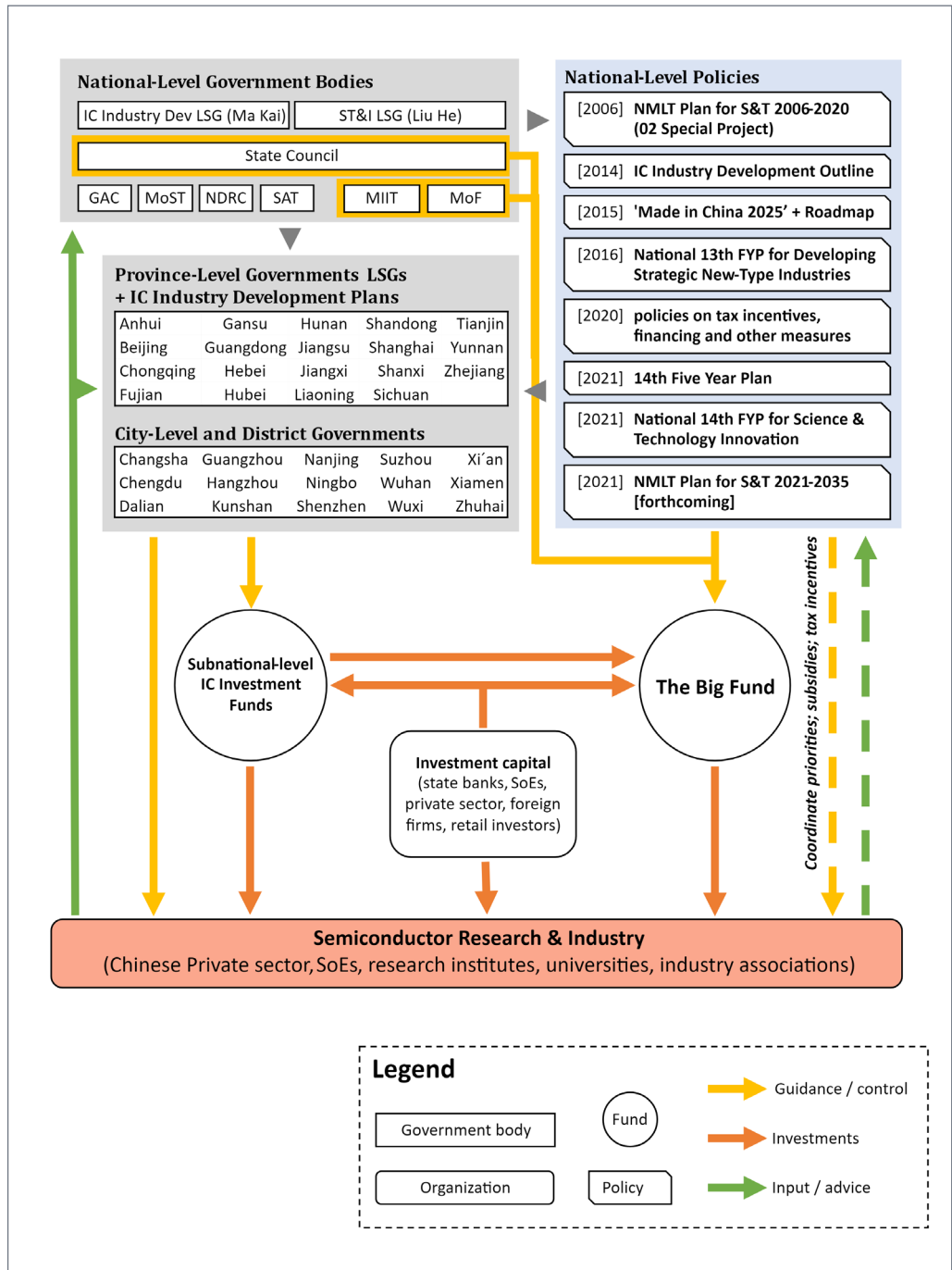


Fig. 3: China's semiconductor ecosystem

The future of China's policy for the semiconductor sector

China's evolving approach to building its semiconductor sector since 2014 has been characterized as a **fast-follower strategy**, which recognizes the structural barriers to reaching the global technological frontier and the advantages of focusing at least initially on lower value-added positions in the global value chain.³² The state aims to let the market “*play a guiding role*,” while keeping its hands on key policy and financing levers. Policies seek to leverage the international value chain and thus, emulate the success of Japan, Taiwan and South Korea. In the 1960s, these countries had been comparable to or even lagging behind China in the IC sector but now occupy much higher value-added positions in the value chain.³³

The key question now is whether China's leaders, facing growing decoupling pressures from the US and its allies, persist with the fast-follower approach or decide to bet on less proven pathways for **accelerated technological catchup and leapfrogging**. There are signs of movement toward the latter approach, although in ways consistent with “proactive integration” into global technological innovation systems, rather than a return to older models of autarkic development. China's **14th Five-Year Plan (FYP)**, released in March 2021, treated semiconductors (unlike the 13th FYP) as an independent category, one of seven frontier technologies prioritized for national breakthroughs.

In May 2021, the MIIT presented to the ST&I LSG about the forthcoming **14th Five-Year Plan for Science & Technology Innovation** (14th FYP S&TI), which will address priorities set in the 14th FYP. The meeting also discussed the **post-Moore era** of semiconductors.³⁴ This refers to alternative materials and techniques that will potentially allow IC design to transcend the growing physical challenges to increasing computing power that are expressed in Moore's Law. Success in such alternative pathways might open up opportunities to leapfrog China's lag in existing processes (to “*change lanes and overtake others*”³⁵) or at least to capture a leading position in emerging markets.³⁶

In this context, the 14th FYP prioritizes “*development of silicon carbide, gallium nitride and other wide-bandgap semiconductors.*” Such third-generation semiconductors are also targeted in IC industry development plans issued by multiple subnational governments. In addition to the 14th FYP S&TI, China is likely to issue a new **National Medium & Long-Term Plan for Science & Technology Development** (NMLTP) during 2021 for the period 2021–2035.³⁷ Since the 02 Special Project was instituted under the previous NMLTP, evaluation of its success and the introduction in 2021 of a new national special project for semiconductors will likely be key elements shaping policy for this sector.³⁸



Situation and prospects for China's semiconductor sector

As of 2020, China's self-sufficiency in ICs (including China-based operations by non-mainland Chinese firms) was estimated at just 16%.³⁹ China's IC imports for the first five months of 2021 rose 30% compared to the same period in 2020.⁴⁰ Unsurprisingly, Chinese authorities now rarely cite the MiC 2025 targets. Greater emphasis is now given to developing China's IC sector as an integrated ecosystem, and underlying resources in which China remains deficient: **R&D capacity and human talent**. This aligns with the general emphasis in the 14th FYP on ongoing improvement of China's innovation resources and systems, including through exchanges with leading foreign firms and experts.

By one 2019 estimate, the entire Chinese semiconductor sector's **R&D spending** was less than that of a single U.S. company, Intel.⁴¹ However, some innovation indices indicate that Chinese actors are increasing their contribution to the global IP pool for semiconductor technologies. For example, semiconductor-related filings with the U.S. Patent and Trademark Office by applicants based in China rose 30% compared to 2020, although they still accounted for less than 10% of total applications.⁴² As Chinese firms spend a share of revenue on R&D comparable to their foreign counterparts, national R&D spending should expand in tandem with the growth of the whole semiconductor industry.

However, low market share in many subsectors limits the progress that many firms can expect to make in R&D spending without assistance.⁴³ This may be partially offset by the reported growing involvement in the sector of well-resourced state-owned entities such as China Electronics Technology Corporation (CETC) and China Railway Construction Group, in addition to the Big Fund's investments.⁴⁴

The *China Semiconductor Industry Association (CSIA)* assessed that as of 2019, around 512,000 people were directly engaged in China's IC sector.⁴⁵ For comparison, the sector would, according to one estimate, have needed 700,000 personnel by 2020 to realize sales of RMB 1 trillion, the approximate target implied by the 2014 Outline.⁴⁶ However, given that actual sales in 2020 of ICs produced in China were barely one seventh of that figure (USD 22.8 billion),⁴⁷ it is questionable whether the sector really faces drastic labor shortages. The *CSIA* assessed in 2019 that overall **labor supply** was keeping pace with demand.⁴⁸

The key constraints are likely to be access to the **cream of the global talent pool** and to **personnel with sufficient practical experience** to perform higher-level functions: those who have "sat ten years on the cold bench" working in the industry, as one Chinese insider put it.⁴⁹ First-hand accounts suggest that mid- and senior-level engineers at semiconductor fabrication plants (fabs) in China are still typically Tai-

wanese, Japanese and Korean expatriates.⁵⁰ Continuing reports of talent-poaching activities targeting Taiwanese and South Korean firms reinforce this picture of a persistent dearth of expertise in mainland China's labor pool when it comes to commercial applications.⁵¹

Domestically trained expertise is also unlikely to substitute soon for top-level talent nurtured at leading firms outside mainland China, particularly PRC citizens who have returned to work in China and Taiwanese; both groups have played a critical role in developing China's semiconductor sector.⁵² Nonetheless, measures are being taken to build up deeper expertise at home. In April 2021, one of China's leading microelectronics schools at Tsinghua University set up a new IC Institute to promote "cross-fertilization of basic research and cutting-edge engineering technology across many fields".⁵³

Despite the government's aspiration to "*let the market play a guiding role*," **state involvement** remains at a level that may significantly distort China's semiconductor sector.⁵⁴ According to one estimate, state-backed firms collected 60% of the RMB 213.6 billion (USD 33 billion) China spent in 2020 on semiconductor industry subsidies.⁵⁵ In Shanghai's recently established Star Market exchange, where a growing number of China's promising IC firms are listing, an estimated 70–80% of investors are state-linked entities.⁵⁶ Even managers of state-linked IC investment funds express doubts about whether these huge sums will be used effectively or wasted, and whether state-led funding will crowd out private investment.⁵⁷

But given that lack of money has been a long-term development constraint for Chinese semiconductor firms, copious funding is probably a net benefit for the sector, especially as Chinese firms can rely on ongoing massive growth in demand for semiconductors. Official statistics show that China's total IC output in May 2021 rose 37.6% compared to May 2020, and that the sector's value-added industrial output grew by 60% in Q1 2021, compared to Q1 2020. In 2020, there were 413 private equity deals in China's semiconductor sector worth a total of RMB 140 billion (USD 21 billion).⁵⁸

In addition to access to foreign technologies and expertise, the **key factors for the future success** of China's IC sector are likely to be (a) how much cooperation and synergies are realized among Chinese firms at different positions in the domestic semiconductor value chain; and (b) how much the sector as a whole can leverage China's world-leading growth in emerging digital technology ecosystems that rely heavily on semiconductors, such as intelligent manufacturing, the Internet of Things (IoT) and self-driving vehicles.

This **whole-ecosystem, demand-led approach** seems to have general support among industry experts and government planners.⁵⁹ China's domestic markets are now large and mature enough to support commercial expansion and technical development. Moreover, the presence of Chinese digital products and firms in foreign markets is unlikely to be completely curtailed by U.S. political pressure.⁶⁰ However, that pressure can only be expected to grow. In addition to general U.S. alarm about China's growing competitiveness in this key field, particular concerns about China's 'civil-military fusion' approach to technology development and military capabilities are gaining ground, as reflected in the stated reasons for existing and proposed U.S. export controls targeting Chinese semiconductor firms.⁶¹

To some extent, this will likely force semiconductor firms worldwide to at least make an appearance of picking national sides.⁶² Even if broad-based decoupling from Chinese industry does not occur, this pressure will have distorting effects on the global value chain. Shanghai's new IC sector development plan describes the situation as follows: "the global supply chain ... is no longer based solely on market mechanisms ... but more on supply chain security and other factors."⁶³



3. Analysis of the production steps

Chip Design (process step)

Chip design is the first step of the production process and results in a design file that is given to a fab for wafer fabrication. Designing different types of chips requires different skills and process flows. One can roughly distinguish among digital, analog, radio frequency (RF) and mixed-signal chips. Designing an analog chip on a 180nm process node is very different from designing a microcontroller on a 40nm process node or a mobile system on a chip (SoC) on a 5nm process node. The design process is very skill-intensive (highly educated talent), relies on high R&D costs and has the highest value-add (around 50%) of all production steps.⁶⁴

A chip design is always based on a process node from a particular company. Foundries release process design kits (PDKs) for their process nodes that are used by chip designers to develop a chip on this process node.⁶⁵ Chips designed on, for example, TSMC's 5nm node cannot be produced on Samsung's 5nm node: Most of the chip would need to be redesigned first. Thus, choosing a foundry and deciding on a process node are often long-term, strategic decisions for chip designers—especially for cutting-edge chips.

Chip designers rely not only on close collaboration with their fabs but also on electronic design automation (EDA) tools and IP providers. EDA tools provide the development environment, and IP vendors supply crucial design blocks, from simple USB interfaces to fully fledged processing cores, to chip designers. IC design service companies also play a crucial role in helping chip designers navigate this increasingly complex ecosystem.⁶⁶

The Market

Worldwide, the number of companies designing their own chips is increasing. The chip design market is becoming more diverse because of the need for application-specific chips, such as artificial intelligence (AI) accelerators. Today, consumer electronics companies, hyperscalers and car makers all develop special-purpose chips to gain a competitive advantage. The **US** has, by far, the largest chip design industry: **U.S.** chip design (“fabless”) and system IC companies⁶⁷ have a market share (sales) of 64%. Second are **Taiwanese** chip design firms, such as *MediaTek* and *Realtek*, with a total market share of 18% and then, **Chinese** firms, such as *HiSilicon* and *Unigroup*, with a total market share of 15%.⁶⁸ **European, South Korean and Japanese** chip design companies have only a miniscule share (around 1% each).



Barriers to Entry

Compared to other segments of the semiconductor value chain, chip design has relatively low market-entry barriers. For smaller startups, the steep licensing fees for EDA tools and IP can be a challenge, and several initiatives try to lower this barrier to entry.⁶⁹ Furthermore, in the past, venture capital tended to focus on software startups more than on chip design companies.⁷⁰

The Chinese government's efforts to increase self-reliance

Using rapid growth in China's chip design sector to drive development of the Chinese semiconductor manufacturing industry was an explicit goal in the 2014 Outline. Growth in global demand for smartphones, with manufacturing concentrated in China, created some comparative advantage for Chinese firms to pursue chip design. With relatively low barriers to entry, Chinese firms rapidly gained market share, although only a few companies, such as *HiSilicon*, *Goodix* (fingerprint sensors) and *OmniVision* (image sensors), have approached the global technological frontier.

Policymakers aim to harness this market-driven success in chip design to pull up firms in other IC sectors with relatively higher entry barriers and lower customer demand, and where previous state-led supply-side efforts have clearly failed, as with EDA tools.⁷¹ Demand-led growth also helps to attract overseas industry leaders to partner with local firms. For example, in 2014 the Taiwanese chip design leader *MediaTek* invested USD 48.9 million in one Shanghai IC fund, with the express goal of leveraging China's semiconductor sector to boost *MediaTek's* global market position.⁷²

The 2014 Outline emphasized driving China's chip design sector to the global front rank in key areas such as network communications and using the sector to accelerate development of emerging fields like cloud computing and the IoT, while “*improving support for deep integration of information technology and industrialization.*” This two-track approach of targeting mature markets and emerging technologies was reflected in the MiC 2025 roadmap, which specified that chip design should focus on applications with high-volume demand (server and desktop computer CPUs, embedded CPUs, memory, FPGAs) and leading-edge activities (SoC, ESL and 3D-IC design).

Subnational governments have also focused on chip design, which is emphasized in multiple policy documents issued within the last two years by province- and city-level governments. Shanghai's Lingang Special Area showcases China's efforts to promote and exploit chip design by co-locating work in this sector with other IC



production steps and R&D activities. The zone incorporates an innovation hub that hosts leading Chinese chip design firms, such as *Cambricon* and *Horizon Robotics*.⁷³

Competitive position of the Chinese industry

The number of IC design firms in China almost doubled from 2015 to 2020, but may suffer from excessive fragmentation. According to one estimate, in 2019 the combined revenue of some 500 Chinese design firms was less than 70% that of U.S. industry leader *Qualcomm*.⁷⁴ Most of the Chinese design sector's products remain, in performance terms, in the middle to lower end of the global market. In 2017, the chief executive officer (CEO) of one Chinese EDA tools vendor expressed the view that many Chinese IC design firms were too immature to use the available investment money effectively.⁷⁵ The reliance of the firms with the highest revenue on the mobile communications market is a potential source of vulnerability as smartphone demand slows with market saturation.⁷⁶

However, Chinese design firms will benefit from Beijing's commitment to promoting multiple fields that support chip design activity, including intelligent manufacturing, the IoT, future telecom networks and artificial intelligence.⁷⁷ These trends have led China's cash- and data-rich internet platform and consumer device giants, such as *Baidu*, *Alibaba* and *Xiaomi*, to invest heavily in chip design.⁷⁸ *Zhaoxin*, a joint venture between the Shanghai government and Taiwan's *VIA Technologies* (the only non-U.S. firm licensed to use *Intel*'s x86 instruction set architecture for CPU design) has developed a CPU series that seems good enough for state agencies trying to reduce exposure to U.S. technology.⁷⁹

This expanding demand is reflected in design firms' success in raising capital. *Horizon Robotics*, for example, recently raised USD 150 million from domestic and international investors, less than two years after the firm's previous funding round raised USD 600 million.⁸⁰ *Horizon* illustrates how Chinese design firms are relatively favored domestically and globally. Investors include *Intel* and **South Korea's SK**, the firm has benefited from Chinese government contacts, and its services are in demand from firms in China's fast-developing self-driving car sector.⁸¹ Chinese analysts also expect the design sector to "share the dividends of IC foundry advancement," as foreign and domestic companies invest in massive foundry expansion across China.⁸²

Likelihood of China catching up within 5 to 10 years

The potential negative impact of U.S. export controls on Chinese IC design firms are reflected in the fate of *HiSilicon*, which since 2019 has suffered plunging revenues



and loss of skilled staff as a result of U.S. export controls. However, as the main beneficiaries of *HiSilicon's* decline appear to be other Chinese firms, the efficacy of such measures to stunt the overall progress of China's chip design sector is questionable. More serious may be the reduced access to top-level human talent nurtured in foreign firms. China's long-running effort to develop secure and controllable infrastructure that depends less on foreign technology may help to drive developments in chip design, as shown by *Zhaoxin's* CPUs.

The scale of expansion in digital applications within China buoys prospects for Chinese chip design firms. For example, China is projected to lead the world in number of 5G connections by 2023.⁸³ *Xiaomi*, *Huawei* and *Alibaba* have developed consumer IoT ecosystems that are driving chip design advances, with *Alibaba* releasing what is reportedly the world's most powerful RISC-V-based processor in 2020.⁸⁴ In electric vehicles (EVs), China accounts for more than 40% of the global market, with China's domestic EV market projected to grow 50% during 2021.⁸⁵ Self-driving technology is linked to EV development, and many industry leaders are investing in this ecosystem's expansion within China.

The key question in this value chain segment is whether Chinese firms can raise their share of the rapidly growing proportion of worldwide semiconductor revenues that is accruing to chip design companies, or whether this growth will be largely captured by foreign fabless leaders like *Nvidia* and *Qualcomm*.⁸⁶ Overall, chip design is probably the value chain segment in which Chinese firms have the best chance of competing at the global technological frontier during the coming decade.

Strategic dimensions

Competitiveness dimension

Rapid growth in fabless design firms' share of global semiconductor **revenues** means that Chinese success in this area could significantly affect the global industry's balance, as more profits are captured in China and flow to firms elsewhere along the value chain. These **spillover benefits** would extend to multiple economic sectors, given the concentration of electronics manufacturing in China and growth in its domestic markets for ICT applications. Relatively low **barriers to entry** mean Chinese success would not by itself imply atrophy of chip design capabilities in other countries. However, the link between design and applications means foreign firms might be pushed out of emerging sectors such as self-driving cars in which the technological ecosystem is advancing relatively faster in China, thus favoring Chinese fabless design firms.



National security dimension

Chip design capabilities are not a key **chokepoint** in the global value chain, as they are distributed internationally and are based on range of factors that are difficult to restrict completely across borders. However, **Chinese** fabless companies, such as *HiSilicon*, *Tianjin Phytium Technology*, *Sunway Microelectronics* and others, have been targeted with export restrictions by the U.S. government. The reason given for these restrictions was that the entities concerned “*are involved in activities that support China's military actors (and) military modernization efforts.*”⁸⁷

These U.S. measures reflect concern about the **military utility** of advanced processor chips, given the expected rise in importance of artificial intelligence and other functions based on computing power in military applications. In this context, the accumulation of design capabilities that support development of such chips has implications for the international military balance. The issue here is not the production step itself but the end products that it supports, in a national adversarial context.

The design process itself is not efficient in enabling **espionage**, given the complexity and resources required to successfully compromise a chip. Thus, the **espionage risk inherent in this production step is very limited**, especially compared to back-end processes like assembly, test and packaging (ATP).

Resilience dimension

Chip design capabilities represent a relatively small risk in this context, as they do not constitute **points of failure** that could compromise the wider value chain or result in significant negative spillovers if disrupted. These capabilities are relatively easily **replicated**, because they require comparatively small capital investments and economies of scale. However, developing a large labor pool in design skills takes years, and most nations would likely struggle to achieve this in isolation.

Electronic Design Automation (input)

Electronic design automation (EDA) tool vendors provide the development environment for chip designers to design, verify, test, validate and simulate their chips. Without access to these highly specialized and increasingly complex software tools, it is nearly impossible to develop modern chips. EDA vendors work closely with foundries to support a fab's process nodes as much as possible, so that chip designers can utilize the nodes' technology features in their chip designs.⁸⁸ Together with research organizations such as imec, EDA vendors also help fabs to research, develop and improve their process nodes.⁸⁹ Furthermore, EDA vendors closely collaborate with equipment vendors in developing future manufacturing equipment.⁹⁰ Last, EDA tools facilitate access to third-party IP suppliers, such as ARM, thus allowing chip



designers to include external IP in their designs.⁹¹ In essence, EDA tools facilitate the close collaboration among all actors across the three production steps: design, fabrication and ATP.⁹²

The market

The EDA market is highly concentrated, with three **U.S.** companies—*Synopsys*, *Cadence* and *Mentor* (acquired in 2017 by the German electronics giant *Siemens*)—capturing around 70% of global revenues for many years.⁹³ Especially for advanced logic chip design, such as processors or mobile system on a chip (SoC), access to these three vendors is paramount. Large chip design companies might use software from all three vendors as each EDA tool might be particularly good in a certain area.⁹⁴ There are many smaller EDA companies, but they do not provide tools for the entire design flow; instead, they focus on one niche.⁹⁵ Additionally, the “Big Three” have very aggressive M&A strategies to stay at the cutting edge.⁹⁶ *Synopsys* alone has acquired more than 50 technologies and companies since 2010.⁹⁷

Barriers to entry

The market-entry barriers are moderate for EDA startups, but challenging the Big Three is extremely hard and highly unlikely within the next five years. Successfully establishing an alternative to *Synopsys*, *Cadence* or *Mentor* faces several challenges. First, EDA vendors spend more than 30% of their revenue on R&D to stay at the cutting edge in a highly innovative and fast-paced value chain.⁹⁸ Second, as the Big Three have been the quasi-standard for more than a decade, chip designers are familiar with these tools and reluctant to change. Third, EDA vendors need very close business relationships with foundries and IP suppliers that take many years to establish.

There are some efforts to “democratize” chip design and lower the barriers to entry and the learning curve for chip designers, such as DARPA’s OpenROAD initiative.⁹⁹ But it is highly likely that cutting-edge chip design will continue to rely on access to the Big Three.

The Chinese government’s efforts to increase self-reliance

The Chinese state began trying to promote domestic EDA tools development during the 1980s.¹⁰⁰ As a result of limited progress, in 2000–2001 IC Design Bases (centers) were set up in seven cities with seed funding from the central government, with the

objective of making EDA tools, including foreign-owned ones, generally available to Chinese firms through licensing rights. This initiative also generally performed poorly, with successful Chinese design firms avoiding the centers' services in favor of options outside mainland China.¹⁰¹ Subsequently, the centers have produced some achievements in chip design (in the case of the Shanghai center, enough to be recently blacklisted by the U.S. government¹⁰²), but they also reinforce the market dominance of foreign EDA vendors by making their tools widely accessible.¹⁰³

EDA tools were initially neglected by the Chinese government's current IC policy phase, and did not appear in the 2014 Outline or the MiC 2025 roadmap. As of mid-2020, less than 1% of the Big Fund's investments were assigned to domestic EDA firms. But this situation appears to have begun changing, as U.S. export controls targeting Chinese firms have highlighted the vulnerability of EDA as a chokepoint. As one example, Phase II of the Big Fund invested 20 times more in the EDA startup *Shenzhen Giga-da* than Phase I did in the long-established domestic EDA vendor *Huada Empyrean*.¹⁰⁴

After *ZTE* was placed on the U.S. Entity List, EDA tools were prioritized in China's 2016 National Informatization Plan. U.S. controls targeting *Huawei* in mid-2020, which expressly identified EDA tools as controlled items, were followed by Beijing's August 2020 semiconductor tax incentive package, which included corporate income tax reductions or exemptions for young EDA firms.

Domestic development of EDA will probably also benefit from its prioritization since 2020 by multiple subnational governments. EDA may benefit especially from attention in Shanghai's new five-year IC development plan, given the city's outsize role in successes within China's chip design and fabrication sectors.

Competitive position of the Chinese industry

The Big Three U.S. vendors accounted for 90% of China's EDA market in late 2020, although Chinese firms offer "*credible tools in several EDA categories*," according to a study commissioned by *Cadence*.¹⁰⁵ However, to date, only one Chinese firm (*Huada Empyrean*) offers tools covering a complete design flow, limited to analog chips. Other Chinese firms concentrate on narrow tool sets.¹⁰⁶ This is reflected in the firms' paltry 10% share of China's EDA market, with leading Chinese design and foundry firms continuing to use the Big Three's tools, although *HiSilicon's* access has been reportedly curtailed by U.S. export controls.¹⁰⁷ Widespread use of pirated tools in China likely harms the Big Three less than local EDA firms, which are incentivized by low sales to distribute their products in more convenient but less secure formats.¹⁰⁸

EDA vendors must also compete for a limited pool of software engineers, with the Big Three and with Chinese technology giants, such as *Alibaba*, *Tencent* and *Huawei*. In 2018, *Huada Epyrean* estimated that of 1500 individuals working in EDA R&D across China, only 300 worked for Chinese research institutions and companies, half of them for *Huada*; the rest worked for the Big Three.¹⁰⁹ In comparison, *Synopsys* alone has around 5000 engineers engaged in R&D on EDA tools.¹¹⁰ *Cadence* and *Synopsys* have invested significantly in operations in China over the last few years.¹¹¹

Consolidation in China's chip design sector may harm Chinese EDA vendors, as Chinese design firms increasingly have the money to access the Big Three's tools.¹¹² The commercial imperatives for design firms to use EDA tools that are in sync with manufacturing developments also incentivize Chinese customers to stick with the Big Three, given the latter's privileged working relationships with leading foundries.

Nonetheless, commercial demand is growing in China for domestically sourced EDA tools, to mitigate the risk if U.S. export controls are expanded. Responding to this demand, three new Chinese EDA vendors were set up in 2020, each founded by or hiring executives and engineers from *Cadence* and *Synopsys*. These firms are backed by Chinese government and major private investors, including *Synopsys* itself.¹¹³ Following the 2019 U.S. export controls targeting *Huawei*, *Synopsys* set up a joint venture (JV) in China, and industry rumors suggest another of the Big Three is planning to establish a Chinese JV.

Likelihood of China catching up within 5 to 10 years

The *Cadence*-commissioned study assessed that Chinese EDA suppliers are well positioned to replace U.S. vendors if the latter are cut off from the Chinese market, noting that these Chinese suppliers' product roadmaps "*aim to provide full-flow offerings for IC design at advanced nodes by 2025.*"¹¹⁴ Although leading Chinese firms are unlikely to prefer domestic EDA suppliers, if that choice is removed by expanded U.S. export controls, the result will likely be growing market share for Chinese EDA vendors in categories of chips with simpler designs and in solutions tailored to Chinese customers.¹¹⁵

But even under these conditions and with abundant funding, **Chinese EDA firms are unlikely to be able to provide solutions for chips at the global cutting edge.** There is also a risk that lavish state-led funding and guaranteed procurement will lead Chinese EDA firms to plateau comfortably at capabilities that trail the global technical frontier, a result with many precedents in different ICT sectors in China.



Another critical factor would be availability of the Big Three's tools despite expanded U.S. export controls. This availability might remain extensive, for several reasons. As EDA tools are software, they can be hacked; *Synopsys* has already sued one Chinese business for such behavior.¹¹⁶ Alternatively, the Big Three might ignore piracy, because even illegal use of their tools in China works against the rise of Chinese competitors. Enforcing U.S. export restrictions on EDA may prove challenging. At least one Chinese firm on the U.S. Entity List reportedly set up a shell company as a front for EDA licenses, and other U.S. vendors might follow *Synopsys* in establishing Chinese JVs to facilitate access to their tools for firms like *Huawei* that have been individually targeted by U.S. export controls.¹¹⁷

Strategic dimensions

Competitiveness dimension

The EDA tools market has **substantial barriers to entry at the cutting edge** but small value-add, the highest R&D margin across the value chain and necessarily deep cooperation with (cutting-edge) fabs. Thus, absent U.S. export controls, it is highly likely that the oligopoly of the Big Three (*Synopsys*, *Cadence* and *Mentor*) in China and around the world will continue. U.S. export controls might create a window of opportunity for new Chinese players to enter the market, but whether they will be able to challenge the Big Three long term, and thus, change the market features, is far from certain.

National security dimension

The Big Three's dominance provides the U.S. government with a **chokepoint within the value chain** that can be exploited through export controls. This chokepoint's utility has already been demonstrated in the case of the export restrictions against *Huawei*. Even if access to EDA tools is obtained through pirated copies or hacking, the need for continual software updates from the vendors to keep the tools useful for cutting-edge applications makes it very difficult for Chinese firms to circumvent this chokepoint. Therefore, it is highly likely that (a) the U.S. government will continue to utilize EDA as a chokepoint, and (b) the Chinese government will increasingly invest in its domestic EDA industry.

Resilience dimension

In contrast to the manufacturing process steps and tangible goods (equipment, chemicals, wafers) whose supply can be disrupted by natural disasters and accidents, supply chain **resilience considerations have little relevance** for EDA software.



Intellectual Property (input)

Intellectual property (IP) plays a critical role throughout the semiconductor value chain. The chip design process, in particular, has become so complex that chip designers rely not only on EDA tools but also on third-party IP suppliers, to avoid having to reinvent the wheel for each product. Modern processors and system on a chip (SoC) need memory interfaces, AI accelerators, power management, security features and wireless connectivity, to name just a few. These functionalities are licensed from third-party IP suppliers for implementation in chip designs.

Suppliers of semiconductor IP have an incentive to make it as easy as possible for chip designers to use their IP. Therefore, the suppliers collaborate with foundries to ensure that IP blocks work on a particular process node.¹¹⁸ The advantage for foundries is that their process nodes become more popular with design customers in tandem with the quality of the IP ecosystem they can offer.¹¹⁹

Being able to utilize third-party IP plays such a crucial role in today's chip designs that DARPA recently started its "toolbox initiative" to streamline access for their researchers to third-party IP suppliers¹²⁰: "*DARPA performers are frequently encumbered by having to negotiate access to tools, IP, and services, and execute complex legal agreements that take the time away from what they do best—advancing science to benefit the nation.*"¹²¹

The market

IP suppliers are somewhat similar to chip design companies: They do not sell entire chips, only functional blocks. As in chip design, many IP suppliers are **U.S.** companies. Among the largest IP suppliers by revenue are *Arm Ltd. (UK)*, *Synopsys (US)*, *Cadence (US)*, *Imagination Technologies (UK)*, *Ceva (US)*, *Silicon Storage Technology (US)* and *VeriSilicon (China)*.¹²² The IP supplier market, in general, is highly competitive and fast-moving.¹²³

A special type of semiconductor IP is **instruction set architecture (ISA)**. The ISA defines the basic design architecture of any processor chip. The most important ISAs globally are x86, ARM and RISC-V.

The proprietary **x86 architecture** is controlled by *Intel (US)*, *AMD (US)* and *VIA (Taiwan)*. Historically, it has been the most important and dominant processor architecture for desktops, laptops and servers. In March 2021, *Intel* stated that it would, for the first time, offer x86 core IP alongside foundry services to other firms seeking to build chips, under *Intel's* recently announced integrated device manufacturer (IDM) 2.0 initiative.¹²⁴



What x86 is to the desktop and server market, the *ARM architecture* is to mobile chips. Essentially, all smartphones and tablets are based on *Arm Ltd.*'s proprietary architecture that the company offers via licenses.¹²⁵ *Apple*, *Samsung*, *Huawei* and *MediaTek* all develop their own mobile chipsets, but they are all based on the *ARM* architecture. In recent years, the *ARM* architecture has spread to almost every vertical, from automotive to industrial applications and super-computers.¹²⁶ This increasing dominance of *ARM* architecture is why parts of the chip design industry are worried about the planned acquisition of *Arm Ltd.* (currently owned by **Japanese SoftBank**) by *Nvidia (US)*.¹²⁷

In contrast to x86 and *ARM*, *RISC-V* is a free and open (non-proprietary) processor architecture. A relatively simpler ISA, *RISC-V* lends itself more than *ARM* architectures to smaller chip design teams and shorter product development cycles, features that may work to the advantage of design firms that are less established than industry leaders but enjoy proximity to large and dynamic markets for developing semiconductor applications (this describes most Chinese chip design firms).¹²⁸ Although *RISC-V* lacks *ARM*'s strong IP ecosystem and development environment,¹²⁹ *RISC-V* has become popular worldwide in recent years, partly due to its flexibility and extendibility.¹³⁰

Barriers to entry

New IP suppliers face relatively low market-entry barriers, when compared to other supplier markets and process steps in the semiconductor value chain. Like chip design, developing semiconductor IP is very skill-intensive with high R&D costs but involves relatively low capital investment.

One exception is ISAs, because of strong lock-ins due to network effects. Software does not automatically work on different ISAs but must be adapted. Thus, no matter how much potential a new ISA has, if programmers are not interested in developing compatible software for the processor, the design is doomed to fail.¹³¹

The Chinese government's efforts to increase self-reliance

Chinese authorities have long recognized the need to improve the nation's human resources for generating IP and IP protection systems to incentivize development, although progress on both fronts has been slow. For the IC sector specifically, the MiC 2025 roadmap emphasized both priorities. The 2016 14th Five-Year Plan for the Development of National Strategic Emerging Industries called for supporting the improvement of services provided by third-party IP enterprises in the IC sector. The

State Council's August 2020 measures addressed IP, while subnational governments' IC industry plans also prioritize IP development and acquisition. One (Chengdu) is giving IC design enterprises 50% subsidies for IP purchases, with specific reference to foundry IP modules and EDA tools.¹³²

ISA has been relatively neglected by government policy for the semiconductor sector. However, in 2018 a *RISC-V* Consortium was established in Shanghai, and the Shanghai government began subsidizing *RISC-V*-based chip development and mass production.¹³³

Competitive position of the Chinese industry

VeriSilicon is often identified as the only Chinese firm that is a significant IP provider: Its IP is used in chips developed by *Google*, *Facebook* and *Amazon*.¹³⁴ In 2019, *VeriSilicon*, which has investment backing from *Intel*, *Samsung* and *Xiaomi*, ranked seventh worldwide for IP license revenue and claimed to be conducting R&D for 5nm processes.¹³⁵

Media reports suggest that *Arm China*, a subsidiary of the UK-based owner of *ARM* architecture, may have moved beyond selling and licensing its parent company's IP to developing its own, including a design that allows Chinese-made chips to run a cryptographic algorithm built by China's State Cryptography Administration. Reportedly, clients for *Arm China*'s IP include *HiSilicon*, and in 2019, *Arm China* claimed it would release three new chip design blueprints annually.¹³⁶

However, a power struggle between the company's CEO, its UK parent and the latter's major investor *Softbank* raises questions about *Arm China*'s prospects, as well as about the wider environment for IP protection (and corporate governance generally) in China. Furthermore, the prospect of *Arm Ltd.*'s (UK) acquisition by the U.S. company *Nvidia* raises the risks to Chinese industry of continuing to rely on *ARM* architecture, although Chinese regulators may deny approval for this acquisition or stall until it falls through.¹³⁷ *Arm Ltd.* (UK) recently assessed that its latest ISA is not subject to U.S. export controls, meaning that at present, Chinese companies can continue to use this architecture for chip design.¹³⁸

Beyond *VeriSilicon* and potentially *Arm China*, Chinese industry commentators acknowledge that domestic firms are still "lagging far behind" in IP, and require years of progressive knowledge accumulation before becoming competitive in this field.¹³⁹ However, *RISC-V*'s potential to support a range of applications, and potentially, to displace *ARM* as the leading ISA in some sectors, may create leapfrog opportunities for China's design firms and the larger domestic ecosystem supporting them to



build up proprietary IP, at least for processors. Chinese design firms have focused on *RISC-V*-based products for some time, and quantifiable results are starting to appear.¹⁴⁰ For example, in 2020 Alibaba released what it claimed at that point in time was the world's most powerful *RISC-V*-based processor.¹⁴¹

Likelihood of China catching up within 5 to 10 years

The skill-intensive nature of IP development for the IC sector means that its growth in China has depended on experienced individuals who returned after working abroad for foreign industry leaders. *VeriSilicon* was founded by such a returnee who built his skills working in the US (other notable Chinese IC firms such as *SMIC* and *Spreadtrum* were also founded by returnees).¹⁴² With growing pressure for technological decoupling, opportunities to gain experience abroad will be increasingly constrained, although this will also become less of an issue as China's IC sector matures.

The Chinese industry's clear deficiencies in IP may become a focus for government authorities' lingering tendency to resort to directive supply-side policy to plug obvious gaps, creating risks of wasted effort and resource misallocation. For example, one of Guangdong's IC sector plans directs the province's research institutions and IC design enterprises to pursue development of "independent IP for sub-28nm processes."¹⁴³ This raises questions about how well informed or realistic the plan's drafters were about Chinese industry's limitations, and where efforts would be most effectively concentrated.

Perhaps the best prospects for the development of Chinese IP lie in the emerging *RISC-V*-based development ecosystem. Because the *RISC-V* Foundation is headquartered in Switzerland, *RISC-V* IP is relatively insulated from potential U.S. export controls, and it is receiving considerable attention from China's chip design sector.¹⁴⁴ China's central role in global electronics manufacturing and rapid build-out of digital infrastructure arguably gives China a good chance to be first in defining the optimal use cases (applications) for *RISC-V* and in scaling them commercially. Nonetheless, *RISC-V* is just one type of IP, and it is nearly impossible for Chinese IP suppliers to provide internationally competitive IP for all or most categories within the next 10 years.

Strategic dimensions

Competitiveness dimension

An internationally competitive domestic IP ecosystem provides **significant spillover benefits**, as it is a prerequisite for successful chip design. This, in combination with



relatively low barriers to entry, makes it likely that China will seek to build more domestic IP suppliers and continue to try to acquire foreign IP vendors. Given the overall situation of China's semiconductor ecosystem and the larger electronics manufacturing sector, in the future there will almost certainly be more internationally competitive Chinese IP suppliers similar to *VeriSilicon*.

National security dimension

Third-party IP poses a **negligible espionage risk** but can be utilized as a **chokepoint** against nations that depend on access to foreign IP suppliers. Because the IP market can be highly concentrated for special types of IP, export restrictions could be effective in limiting foreign firms' chip design capabilities. Therefore, China's deficient position in IP is a vulnerability, although the importance of China's markets provides some counter-leverage. For example, many observers expect the **U.S.** firm *Nvidia's* acquisition of *Arm (UK)* to be effectively blocked by Chinese regulators, dampening prospects for U.S. export controls to cut off Chinese access to *Arm's* ISA.

Resilience dimension

Similar to EDA, as a software component in the semiconductor industry, IP has **little to no impact** on the supply chain's overall resilience.

Wafer Fabrication: The Front-End (process step)

In a fabrication plant ("fab"), the chip design is transferred onto a wafer. This process is called "wafer fabrication" or "front-end." Wafer fabrication is conducted in a clean room with the strictest contamination requirements.¹⁴⁵ Fabrication can consist of more than 1000 process steps, involving around 50 different types of manufacturing equipment and up to 400 different chemicals and materials.¹⁴⁶ Cutting-edge wafer fabrication also consumes a lot of electricity and water.¹⁴⁷ Thus, fabs depend substantially on a multitude of equipment, chemical and wafer suppliers, predominantly from the **US, Japan, Europe and Taiwan**.

Fabs are operated by either an integrated device manufacturer (IDM) or a foundry. An IDM designs, manufactures and sells chips by itself. Examples are *Intel (US)*, *Infineon (EU)* and *SK Hynix (KR)*. A foundry offers contract manufacturing to chip design companies that do not own fabs, such as *Apple (US)*, *Huawei (CN)* and *MediaTek (TW)*. Foundries have an incentive to make it as easy as possible for chip design companies to use the foundries' process nodes. To that end, foundries work closely with EDA vendors and IP suppliers.

All fabs aim for high yield and utilization rates. Yield is the share of working chips on a wafer after the fabrication process.¹⁴⁸ When fabs switch to a new manufactur-

ing process, the yield rates are typically low and must be quickly improved to make the process economically profitable. The utilization rate is the amount of time the equipment is used to manufacture chips.¹⁴⁹ Front-end fabs have to run 24/7 to ensure very high utilization rates to recuperate the high investment costs within a few years.

Wafer fabrication differs depending on the type of semiconductor. Logic semiconductors, such as general-purpose processors, graphic chips and AI accelerators, rely on increasingly complex fabrication processes to squeeze more transistors on a square millimeter of wafer so that more complex and powerful chips can be designed.¹⁵⁰ This development, often referred to as “node scaling” or “More Moore scaling,” led to a tenfold increase of transistors per square millimeter in the past 10 years.¹⁵¹ Thanks to “More Moore scaling,” today’s 3nm process nodes can produce significantly smaller transistors than 28nm process nodes in 2011. Mature nodes, which are not subject to constant innovation and increasing complexity, are also essential to the market. In the following analysis, we focus on cutting-edge and trailing-edge wafer fabrication for logic chips.

The Market

Because of the economics of node scaling (skyrocketing fab costs paired with stupendously complex manufacturing processes), many companies dropped out of this “More Moore race.” The number of companies operating **cutting-edge fabs** dropped from almost 30 in 2001 to 2 in 2021.¹⁵² Currently, only *Samsung (KR)* and *TSMC (TW)* successfully operate 5nm fabs. *Intel* struggled in recent years to stay at the cutting-edge but plans to compete again at 7nm and below.¹⁵³ The customers of *TSMC*’s and *Samsung*’s most advanced process nodes are mainly U.S. chip design companies (more than 80% of estimated capacity), such as *AMD*, *Apple*, *Nvidia* and *Qualcomm*.¹⁵⁴ *Samsung*¹⁵⁵ and *TSMC*¹⁵⁶ plan to invest substantially in fabs in the US within the next three to five years, but until then, cutting-edge wafer fabrication is available only in Taiwan and South Korea. Even after *Samsung*’s and *TSMC*’s investments in the US, the majority of cutting-edge wafer fabrication capacity globally will most likely remain in **Taiwan** and **South Korea**.¹⁵⁷

In comparison, **trailing-edge wafer fabrication** (process nodes at 10nm and above) is less consolidated in terms of companies and less geographically concentrated. In addition to *TSMC* and *Samsung*, *UMC (TW)*, *Globalfoundries (US)*, *SMIC (CN)* and *Huahong (CN)* operate process nodes at 14nm and above. Although 28nm nodes were introduced a decade ago, these trailing-edge fabrication processes are still in high demand for applications such as automotive, industrial, the IoT and many more, because designing and manufacturing chips on these nodes are significantly cheaper than at the cutting edge.¹⁵⁸

In general, **Taiwan**, **South Korea** and **China** established themselves as fabrication hubs, with the latter also as a hub for foreign IDMs and foundries, not least because of substantial government support in the form of investment incentives and loans at below market rates.¹⁵⁹ The U.S. Semiconductor Industry Association (SIA) estimates that the 10-year total cost of ownership of a new fab is 30% higher in the US than in Singapore, South Korea or Taiwan and even 37–50% higher than in China. Around 40–70% of this cost differential is due to government support.¹⁶⁰

Barriers to Entry

Cutting-edge wafer fabrication has some of the highest barriers to entry compared to the other process steps in the semiconductor value chain. Skyrocketing capital investments led to cutting-edge fabs costing around USD 20 billion (80% of that are equipment costs).¹⁶¹ In early 2021, *TSMC* announced¹⁶² that it would invest USD 100 billion over the next three years, and *Samsung* plans to invest USD 151 billion by 2030 in its logic chip and foundry capacity.¹⁶³ But cutting-edge wafer fabrication is more than just a money game. Fabs need extensive process knowledge to achieve and sustain high yield after they introduce a new process node. They collaborate closely with research institutes such as imec in Belgium, equipment manufacturers and chemical suppliers to develop new process technologies that are constantly advancing the industry's cutting edge.¹⁶⁴ As long as More Moore scaling continues, market-entry barriers will be insurmountable. Therefore, it is highly likely that *TSMC* and *Samsung* will continue to be the dominant and perhaps even the only cutting-edge foundries. Only *Intel* could become a third player if they are able to establish a successful foundry business.¹⁶⁵

Trailing-edge wafer fabrication has lower barriers to entry, but they are still substantial compared to the other process steps. One challenge is the high demand for manufacturing equipment, as all major foundries and IDMs plan to expand their fabs. Lead times for new equipment can be 18 months, and even used equipment is scarce and increasingly expensive.¹⁶⁶ Entering wafer fabrication, even at the trailing edge, means significant capital investment and establishing a supplier network for materials, chemicals and equipment.

The Chinese government's efforts to increase self-reliance

Throughout the 1990s, China tried to upgrade its fabrication technology through a hands-on state policy, which aimed to develop domestic IP through joint ventures with foreign industry leaders and reliance on China's domestic markets. A combination of these efforts' poor results, obligations to liberalize the sector that came with



China's entry into the World Trade Organization and relaxation of U.S. export controls towards China meant that during the 2000s, China's front-end fabrication sector developed mainly through direct operations by foreign and Taiwanese industry leaders, and the growth of one relatively successful Chinese foundry firm that was started by a Taiwanese engineer (*SMIC*).¹⁶⁷

The 2014 Outline declared that mass production by Chinese firms at 32/28nm process nodes should be achieved by 2015, and at 16/14nm nodes by 2020, with the latter goal reiterated in the MiC 2025 roadmap. The 2014 Outline directed that the Big Fund's initial investments should prioritize fabrication, and almost half of its Phase I investments were assigned accordingly, with another 15% or so committed to categories (materials and SME) that directly support fabrication.¹⁶⁸

By 2019, Chinese media reports suggested that Phase II would focus less on fabrication, and in April 2021, the Big Fund trimmed its holding in *SMIC*.¹⁶⁹ Fabrication is also not targeted in the latest group of subnational governments' IC development plans, except in the case of specialty products and advanced processes. However, Chinese firms however are expanding fabrication capacity massively at mature nodes, with an estimated USD 160 billion of investment in fabs planned over the next five to seven years.¹⁷⁰

Chinese planners have also targeted memory chips, whose relatively lower complexity of fabrication provides a more accessible path to technical upgrading, and where Chinese players can benefit from continuing massive growth in demand due to the boom in digital devices and infrastructure throughout China and the world.¹⁷¹ Chinese memory maker *YMTC* (a product of the Wuhan city government's long-term commitment to developing a local fabrication sector, mergers with other Chinese firms and technology licensing from foreign industry leaders) is developing current-generation NAND technology.¹⁷² However, to date, the yield rates and market share achieved by *YMTC* remain very low.¹⁷³

Competitive position of the Chinese industry

Measured against the 2014 Outline's goals, which admittedly were highly ambitious, China's progress has been lackluster. *SMIC* is the only **Chinese** firm with a 14nm process, but more than 90% of *SMIC*'s revenue comes from mature nodes at 40nm and above. The next-leading Chinese foundry (*Huahong*) has yet to progress beyond 28nm. In contrast, global leader *TSMC* earns nearly half its revenue from 7nm and 5nm nodes, and the firm is commencing risk production with its 3nm node in 2021.¹⁷⁴ Contrasting with the MiC 2025 goal of 40% self-sufficiency by 2020, China-located fabrication in 2020 accounted for less than 16% of China's IC consumption, a num-



ber forecast to rise by only 3.5% by 2025. Furthermore, domestic firms produced barely a third of this China-based output; the rest was produced by foreign and Taiwanese firms.¹⁷⁵

This dominance of non-mainland Chinese firms in China's fab market has attracted national concern. There was a vigorous debate in early 2021 over *TSMC's* expansion of its 28nm fab in Nanjing. Some Chinese commentators argue that such "dumping" will squeeze out local foundries, while others argue that expanded capacity is justified by demand and will help local chip design firms turn designs into products.¹⁷⁶ But even with huge capacity expansion (28 fabs were under construction in 2020, mostly Chinese firms¹⁷⁷) China-based IC production is forecast to reach only 7–10% of the global IC market by 2025.¹⁷⁸ However, China's share is significantly larger at less sophisticated technological levels. In 200mm wafers, for example, China-based fabs accounted for 16% of global capacity.¹⁷⁹

Even if policy ambitions are trimmed to expanding production capacity at mature nodes to serve China's booming demand for various types of chips, the amount of investment funding now available creates potential for waste on a grand scale in the fabrication sector, given its capital-intensive nature and local governments' readiness to support the building of foundries that may not contain proven process technologies. The recent collapse of Wuhan-based *HSMC's* "7nm" project, involving astounding levels of fraud and embezzlement, shows the risks of relying on investment-led progress in such a technically complex field.¹⁸⁰

Likelihood of China catching up within 5 to 10 years

Fabrication is the one production step where, barring a major technological gamechanger, Chinese firms have no prospect of competing on level footing with the global leaders. The lag between China's leading foundry *SMIC* and industry leader *TSMC* is often estimated as at least five years, an assessment recently endorsed by *TSMC's* founder.¹⁸¹ *SMIC's* inability to acquire Dutch firm *ASML's* EUVL technology—a problem that *SMIC* faced even before the firm was included on the U.S. Entity List—severely constrains the firm's prospects of commercializing a 7nm process node. One of *SMIC's* co-CEOs claimed in December 2020 that the firm was ready to introduce mass production at 7nm by April 2021. However, in a February earnings call, the other co-CEO said that U.S. licenses are still needed for equipment to expand production at mature nodes.¹⁸²

Even at 10nm, *SMIC's* ability to achieve mass production is uncertain if the firm is constrained from importing older-generation lithography equipment (DUVL), as was recently advocated by the U.S. National Security Commission on Artificial Intelli-



gence.¹⁸³ In contrast, in May 2021, *TSMC* claimed a breakthrough in developing a future 1nm process.¹⁸⁴ *TSMC* and *Samsung* together are projected to account for 43% of capital investment in fabrication worldwide in 2021,¹⁸⁵ with *TSMC* alone spending USD 30 billion, most of which is assigned to leading-edge nodes.¹⁸⁶

Huawei is reportedly engaged in a venture with the state-owned Shanghai IC Design Centre to build a “de-Americanized” fab, aiming for production at 28nm by the end of 2021 and 20nm by the end of 2022. Even if *Huawei* achieves these goals, it is doubtful whether such a fab could produce commercially competitive chips or would extensively employ domestically produced SME. One analysis claims that a fab using only Chinese equipment is unachievable before 2026.¹⁸⁷ Chinese firms not yet targeted by U.S. controls are likely to be engaged in costly risk mitigation efforts. For example, *YMTC* has reportedly dedicated years and hundreds of personnel to audit its supply chain and try to replace US-based suppliers.¹⁸⁸

Although it is nearly impossible for China to compete with cutting-edge foundries within the next 10 years, China's share of trailing-edge wafer fabrication will almost certainly continue increasing. China's prospects for scaling up competitive domestic firms (*YMTC* and *CXMT*) in advanced memory chip fabrication are notably better.¹⁸⁹ Last, China's leaders now seem to be focused on “post-Moore disruptive technologies”: using non-silicon materials and new fabrication paradigms for performance gains.¹⁹⁰

Strategic dimensions

Competitiveness dimension

The rise of the foundry business model streamlined the division of labor between chip designers and contract manufacturers to the point that there are **very limited spillover benefits (commercially)** for domestic foundry capacity. Although the global foundry market is expected to grow to nearly USD 100 billion by 2025,¹⁹¹ only cutting-edge foundries (meaning *TSMC*, *Samsung* and possibly, *Intel*) enjoy high profit margins and therefore, benefit from **significant revenue capture**. The lack of benefits combined with **increasingly high barriers to entry** (not just at the cutting edge) explain why governments' pushes for domestic wafer fabrication are not commercially motivated. China's efforts to promote domestic fabrication are driven by the threat of U.S. restrictions on inputs to fab production hobbling the capabilities of Chinese firms across a range of applications.

National security dimension

There is a **limited risk of espionage** during wafer fabrication. Implementing a “hardware backdoor” during the back-end processes is much more efficient and effec-



tive. Advanced wafer fabrication capabilities also impact **military utility**, as armed forces generally rely on domestic fabs. Most military-use chips are still made at trailing-edge nodes, but future uses such as AI functions might need cutting-edge fabrication. This explains the U.S. government's placement of *SMIC* on the U.S. Entity List in December 2020: “*Items uniquely required to produce semiconductors at advanced technology nodes 10 nanometers or below will be subject to a presumption of denial to prevent such key enabling technology from supporting China's military modernization efforts.*”¹⁹²

Resilience

Because cutting-edge wafer fabrication is limited to Taiwan and South Korea, increasing the resilience of the manufacturing supply chain by diversifying fabs geographically has strategic importance for several governments. Cutting-edge wafer fabrication constitutes a **concentrated point of failure** in case of natural disasters or geopolitical conflicts with **severe spillover damage** in many industries, shown by the current “chip crunch” affecting the automotive manufacturing sector. **But barriers to replicability** make it highly unlikely that cutting-edge fabrication will move away significantly from Taiwan and South Korea for many years. Resilience would be increased to some extent by the fabs *TSMC* and *Samsung* recently announced that they would build in the US, but *TSMC* has made clear that most of its investments and its most advanced process nodes will remain in Taiwan.

Equipment (SME) (input)

Semiconductor manufacturing equipment (SME) can be roughly divided into two categories: front-end equipment for wafer fabrication and back-end equipment for assembly, test and packaging (ATP). The front-end (wafer fabrication) can consist of more than 1000 production steps. Therefore, today's fabs rely on roughly 50 different types of highly specialized manufacturing equipment.¹⁹³ Even the largest SME suppliers specialize in developing equipment only for certain production steps, such as deposition, lithography, cleaning or process control. Thus, to successfully set up a process node, fabs need equipment from a variety of suppliers. Wafer fabrication equipment vendors have close research collaborations with fabs, chemical suppliers and research organizations. Generally speaking, back-end equipment is less complex and less expensive, and the back-end consists of fewer process steps resulting in fewer types of equipment and thus, significantly lower investment costs for a new back-end fab.



The market

Although there are many different SME suppliers, the equipment necessary for each manufacturing step is often controlled by only a very few companies, resulting in a highly concentrated market for certain types of equipment.¹⁹⁴ The largest SME suppliers by revenue are *Applied Materials*, *KLA* and *Lam Research* in the **United States**, *Tokyo Electron* in **Japan** and *ASML* in the **Netherlands**. *ASML* is the only supplier for the most advanced type of lithography equipment, necessary to manufacture chips below 7nm. *Tokyo Electron* holds more than 90% of the photoresist processing market.¹⁹⁵ *Applied Materials* controls most of the market for deposition and doping equipment.¹⁹⁶

The global SME market grew from USD 22 billion in 2003 to around USD 69 billion in 2020.¹⁹⁷ Not surprisingly, the countries with the highest investments in fab capacity (**South Korea, Taiwan and China**) are also the most important sales markets for SME suppliers. In 2020, the three countries together accounted for 73% of equipment sales.

Barriers to entry

How hard it is to enter the SME market and successfully compete with the market leaders depends on various factors. First, SME suppliers have significant R&D costs; R&D margins are typically 11–16%. Second, especially for the most advanced types of equipment, such as extreme-ultraviolet (EUV) lithography, suppliers rely on a vast supply chain (in the case of *ASML*, more than 5000 suppliers).¹⁹⁸ Third, SME suppliers have very close, decades-long business relationships with fabs. That said, there are types of equipment, especially in the back-end, that are easier to manufacture and thus, lower barriers to entry for new companies. However, compared to other process steps and inputs in the semiconductor value chain, front-end equipment certainly has among the highest market-entry barriers.

The Chinese government's efforts to increase self-reliance

The 02 Special Project, instituted in 2009, aimed to generally localize required equipment for 90nm processes, develop equipment prototypes for 65nm and make technological breakthroughs for 45nm and below.¹⁹⁹ The MiC 2025 roadmap directed that Chinese enterprises should reach the “*international first echelon*” by 2030 in process equipment at nodes of 90nm and below, and in lithography technology including EUV. IC equipment was also prioritized in the 13th Five-Year Plan for S&T Innovation (2016–2020), which listed goals including 14nm etching equipment and 28nm



immersion lithography machines.²⁰⁰ The 14th Five-Year Plan (2021–2025) summary released in March 2021 listed R&D in IC priority equipment and breakthroughs in IC advanced industrial processes among key challenges to tackle in frontier S&T fields.

The imperative to import substitute SME increased sharply when U.S. export controls were introduced in 2020 targeting *Huawei* and *SMIC*. The declared intention for the Big Fund's Phase II is to provide “*a sustained high level of support*” for development of specific SME categories.²⁰¹ In 2020, Beijing instituted significant tax relief for firms engaged in semiconductor manufacturing at nodes of 65nm and below.²⁰² This was followed in March 2021 with the suspension of import taxes until 2030 on certain SME parts and materials where the domestic industry cannot provide the required performance.²⁰³

Subnational governments have also focused on SME development in multiple IC development plans over the last two years. Shanghai's 2021–2025 IC plan, for example, includes supporting R&D and industrialization for “*12-inch high-end etching, cleaning, ion implantation, lithography, thin film, wet process, heat treatment and optical measurement equipment.*”²⁰⁴ Shanghai's Lingang Special Area for developing the IC industry includes a bonded manufacturing zone, where components can be imported duty-free.²⁰⁵

Chinese authorities also seem to have pushed largely unsuccessful foreign M&A attempts in the SME sector. The stymied 2016 bid by Fujian Grand Chip for the German equipment maker *Aixtron*, for example, was backed by the Big Fund and linked to various Chinese state-owned enterprises and government agencies.²⁰⁶

Competitive position of the Chinese industry

The U.S. export control measures targeting *Huawei* and *SMIC* have highlighted the dependence of China's semiconductor industry on foreign SME. In mid-2020, a former director of China's Ministry of Industry and Information Technology said that 90% of Chinese industry's SME needs were imported.²⁰⁷ According to one foreign estimate in early 2021, China's SME sector met less than 8% of the Chinese industry's demand, with “*little to no capacity to build (for) photolithography, wafer inspection, advanced ion implantation, atomic layer etching, and testing advanced logic chips.*”²⁰⁸

The global market share of Chinese SME vendors in 2019 was estimated at less than 2% in every major category except equipment for packaging and test.²⁰⁹ Except for *Naura* and *AMEC*, in 2020 Chinese SME vendors had revenues of less than USD 150 million²¹⁰; for comparison, one U.S. firm (*Applied Materials*) reported USD 17.2 billion

revenue in fiscal 2020.²¹¹ A survey in early 2021 of 10 leading Chinese SME vendors revealed that only one (*AMEC*) was making products for sub-14nm processes, although many offered products for 28nm processes.²¹² Most equipment produced by Chinese firms goes not to wafer fabs but to semiconductor ATP, and to manufacturing of solar panels and flat-panel displays.²¹³

In May 2021, Chinese media claimed that for 22–45nm processes, the nation had achieved the technical capability to substitute for foreign sources in SME, excepting photolithography.²¹⁴ In this production step, China's foreign dependence extends well beyond the cutting-edge process nodes for which *ASML* is the sole supplier. The one notable Chinese supplier, *SMEE*, has achieved mass production only at 90nm. The firm aims to commercialize a 28nm machine as early as Q4 2021. *SMEE* is reportedly the government's bet to eventually substitute for *ASML*, *Canon* and *Nikon*.²¹⁵ In 2020, a Chinese state institute published internationally peer-reviewed research indicating progress in 5nm laser lithography, but by the researchers' own admission, this remains "far away" from production technology.²¹⁶

Chinese firms are now reportedly trying more systematically to switch to domestic SME suppliers to mitigate the risk of new U.S. measures further cutting off access to foreign sources, partly due to pressure from Chinese authorities to do so.²¹⁷ However, according to one estimate, in 2020 Chinese firms reduced their purchases of US-sourced equipment by 16% foreign SME vendors continue to see strong sales growth in China.²¹⁸ In 2020, China became the largest market globally for SME sales, growing by 39%.²¹⁹

Likelihood of China catching up within 5 to 10 years

Although the Chinese industry still has miniscule market share, significant basic research progress seems to have been achieved, and Chinese firms have some presence in every SME category.²²⁰ In this context, the picture could change significantly over the decade with scale production rolled out by domestic firms in some SME categories, particularly with involvement of well-resourced state-owned conglomerates like *CETC*. However, even if Chinese SME vendors catch up in certain types of equipment (more likely in the back-end than in the front-end), it is nearly impossible for China to "de-Americanize" within this decade across the dozens of types of equipment necessary for wafer fabrication.

In May 2021, research progress on immersion lithography equipment (necessary for Chinese lithography to advance below 90nm) was reported by Chinese media as in a "state of steady progress," suggesting that near-term breakthroughs are not expected. EUVL development (critical for commercial-scale production below 14nm) has



also progressed in some aspects but remains far from manufacturing implementation.²²¹ Even with a well-resourced and coordinated national R&D effort to achieve functional EUVL, it remains many years away given the number of complex systems that must be developed and integrated, barring technical assistance from foreign industry leaders.²²²

Strategic dimensions

Competitiveness dimension

Increasing the competitiveness of China's SME suppliers is important to the Chinese government because of **significant spillover benefits**. Chinese fabs today face a dilemma: Relying on US-origin SME creates business continuity risk, due to potential export restrictions relying. However, on currently far inferior Chinese-origin SME results in lower yield and lower utilization, making it impossible to compete internationally even at mature nodes. An internationally competitive domestic SME industry would allow Chinese-owned fabs to "de-Americanize" faster and thus, significantly reduce risk from U.S. export controls. Therefore, Chinese government authorities will continue to focus on supporting China's SME industry despite (in fact, precisely because of) **substantial barriers to entry**, especially for cutting-edge front-end equipment, such as EUV lithography.

National security dimension

SME is an effective **chokepoint** vis-à-vis China as shown by U.S. export controls targeting *Huawei*, although Chinese progress with import substitution might progressively ameliorate this issue. Restricting the export of certain types of SME to curb adversaries' technological progress has a long history in the US.²²³ Today, the Wassenaar Arrangement lists around 20 types of SME that fall under the dual-use regulation for which member states impose export restrictions.²²⁴

Although there is **neither a direct espionage risk** nor **immediate military utility** from SME, the national security dimension (limiting an adversary's technological advancements) is the main motivation for SME export controls. In this context, the U.S. National Security Commission on Artificial Intelligence recently recommended internationally coordinated restrictions on export to China of SME for process nodes at 16nm and below, to impede development by China of AI-based military capabilities.²²⁵

Resilience dimension

Cutting-edge front-end SME in some ways constitutes a **concentrated point of failure** with potentially **significant spillover damage**, but disruptions in the supply chain typically do not have an immediate impact, because the supply is not consumable.

Foundries and IDMs acquire SME only when building or upgrading a fab. Thus, compared to consumable supplies such as chemicals or wafers, the resilience of the international SME supply chain is less of an issue for governments than industry competitiveness and adversarial actions by national rivals. Barriers to entry mean that **replicating SME production domestically** is unattractive, unless conditions align to attract foreign industry leaders. Taiwan's government, for example, is trying to leverage the island's dominance in fabrication to persuade foreign SME vendors to locate business activities in Taiwan.²²⁶

Chemicals and Materials (input)

The semiconductor industry relies on an extensive number of chemicals and materials for wafer fabrication (front-end) and assembly, test and packaging (back-end). The whole manufacturing process utilizes as many as 400 chemical products, many of which are protected by trade secrets.²²⁷ To ensure node shrinkage, highly pure chemicals, gases and materials are necessary; contamination requirements are often in the range of a few parts per trillion (ppt) with dozens of control parameters.²²⁸ Generally speaking, during assembly, test and packaging, fewer chemicals are used, and the purity requirements are less strict than during wafer fabrication. Front-end fabs rely on materials such as photomasks and photoresists, specialty gases and wet chemicals. Back-end fabs rely on organic substrates, ceramic packages, resins, and bonding wires.²²⁹ Chemical suppliers closely collaborate with equipment vendors and fabs during research and development. As fabs depend on a steady supply of highly pure chemicals, chemical suppliers undergo an extensive quality control process before being allowed to supply chemicals to a specific foundry or IDM.²³⁰

The market

Because of the range of materials necessary for the semiconductor production process, there are dozens of different suppliers most of which are in **Japan**, the **United States** and **Europe**. Yet the market can be highly concentrated when looking at chemicals for particular process steps. For example, three **Japanese** EUV photoresist suppliers (*Tokyo Ohka Kogyo*, *JSR* and *Shin-Etsu Chemical*) have a combined market share of more than 90%.²³¹ Moreover, as photoresists are fine-tuned for specific production processes fabs often single-source photoresists.²³² However, like the rest of the chip industry, chemicals and materials are always evolving, not just to ensure node shrinkage but increasingly also in the back-end for advanced packaging.

Barriers to entry



The market-entry barriers vary depending on the chemical or material and production process step. The purity requirements for materials used during assembly, test and packaging are less strict, and new suppliers might have an easier time entering this market. The highly pure wet chemicals and gases needed for wafer fabrication are often produced by large suppliers, such as *BASF*, *DuPont*, *Air Liquide* and *Shin-Etsu*. For smaller suppliers, barriers to entry are high. It is hard to achieve the necessary economies of scale to constantly invest in better purification mechanisms in their plants to ensure the necessary levels of purity for electronic-grade chemicals.²³³

The Chinese government's efforts to increase self-reliance

Materials development was emphasized in the 02 Special Project.²³⁴ Photoresists were prioritized in the 2014 Outline and in the 14th FYP (March 2021), and photomask materials in the MiC 2025 roadmap. Materials generally, including many specific categories like photoresists, “high-purity chemicals” and “high-end electronic chemicals,” are emphasized in the current IC development plans of several subnational governments, always in the context of developing a wider IC production cluster and value chain. The tax relief measures introduced nationally in April 2020 and March 2021 include import tariff exemptions for raw materials that “cannot be produced domestically or whose performance cannot meet their needs,” with specific reference to photoresists and photomasks.

The Big Fund's Phase II is reportedly prioritizing investments in cleaning and chemical grinding equipment.²³⁵ National and subnational-level industry plans also focus on development of compound semiconductor materials, such as silicon carbide and gallium nitride, a developing field that seems to be receiving attention from senior national leaders.²³⁶

Competitive position of the Chinese industry

In early 2021, one expert assessed that Chinese firms still lagged in critical materials, such as IC-grade polysilicon, EUV materials and photoresists.²³⁷ However, the research efforts driven by the 02 Special Project have helped Chinese firms progress toward limited capacity for import substitution in this sector, although not toward near-term global competitiveness. For example, in 2020 the Chinese firm *Nata Optoelectronic Materials* produced an argon fluoride (ArF) photoresist material that passed tests for use in 50nm processes. Although this achievement is notable, this product is unlikely to support viable production by Chinese fabs at sub-50nm nodes, and very unlikely at sub-10nm.²³⁸ In January 2021, another firm (*Suzhou Crystal*



Clear Chemical) imported equipment that the firm claims will allow it to produce photoresists on a large scale for use at 45–28nm nodes within three years.²³⁹

China has one potential advantage in materials: global dominance in extraction and processing for critical minerals used in the semiconductor value chain. For rare earths, one April 2021 study estimated that of the 17 rare earth elements, China led in extraction for 9 and in refining for 14. Although steps are being taken by the US, Australia and Japan to reduce Chinese dominance, China remains the primary source for rare earths used in memory, logic and analog semiconductors.²⁴⁰ China also accounts for 80% of the world's supply of tungsten, another mineral critical for semiconductor production, and 60% of the global semiconductor industry's consumption of fluorspar.²⁴¹

Likelihood of China catching up within 5 to 10 years

Chinese suppliers should benefit from the vast amounts of funding now available for anything semiconductor-related and efforts by subnational governments to promote materials production in integration with other value chain segments—especially in Shanghai, the most promising hub of China's semiconductor industry. Thus, for types of materials with less strict purity requirements especially in the back-end Chinese suppliers most likely will play a stronger role over the next years. For high-performance materials used in cutting-edge wafer fabrication, the market-entry barriers are substantial. It is unlikely that Chinese suppliers will be able to successfully enter this market segment and challenge international incumbents within the next 10 years.

In critical minerals, China is unlikely to exploit its dominance to the advantage of its domestic semiconductor materials sector in view of the international blowback that this would cause. However, in a worsening geopolitical climate, this action cannot be completely ruled out.

Strategic dimensions

Competitiveness dimension

There are **significant barriers to entry** for production of cutting-edge front-end chemicals. However, there are also **strong spillover benefits** for China from raising the international competitiveness of Chinese chemical suppliers. The main such benefit is to become less reliant on U.S. chemicals suppliers and thus, “de-Americanize” semiconductor manufacturing, similar to import substitution efforts in China's SME sector that are motivated by risk of additional U.S. export restrictions. In this



decade, it is highly likely that Chinese suppliers will be able to increase their global market shares for bulk chemicals and materials with less strict purity requirements.

National security dimension

There is **no espionage risk** from chemicals and **very limited military utility**, but several chemicals constitute a **chokepoint** that can be exploited through export restrictions. The export of various etching gases, photoresists and masks has been restricted for a long time. For example, U.S. suppliers need a license to export these materials to China.²⁴² Chokepoint exploitation has not been limited to China. In 2019, the Japanese government restricted the export of key chemicals (photoresists, etching gases, hydrogen fluoride) to South Korea without an export license.²⁴³ This led South Korea to invest significantly in its own capacity to produce these chemicals.²⁴⁴

Resilience dimension

There is potential for significant **spillover damage** from this sector, because fabs depend on a steady supply of chemicals and materials sourced from a global supply chain with **concentrated points of failure**. Several semiconductor materials are currently in short supply due to natural disasters, fires in production plants, increasing demand due to the COVID-19 pandemic and lack of economic incentives to immediately increase production capacity.²⁴⁵ This shortage has contributed to constraints on the global supply of semiconductors, affecting many industrial sectors worldwide.

Entry barriers to **replicating** production of high-end chemicals create obstacles to diversifying the global value chain in this field, although particular governments may be able to leverage existing advantages in other steps of the value chain. For example, Taiwan is trying to leverage its dominance in fabrication to attract foreign industry leaders in other processes and inputs. For critical minerals, the prospects for significantly diversifying the global supply away from China remain uncertain over the next decade, although the US and some of its allies are investing considerable resources toward this goal.²⁴⁶

Wafers (input)

Wafers form the basis of semiconductor manufacturing, and fabs rely on a steady supply of highly pure and highly plane wafers. The equipment for a fab's process node is designed for wafers with a specific diameter, such as 300mm, 200mm or 150mm. Wafers use various materials. The most important one, by far, is silicon (Si). Apart from silicon wafers, there are "compound" wafers, such as silicon carbide (SiC), gallium nitride (GaN) and gallium arsenide (GaAs). Because the physical properties of these wafers differ from those of silicon, these materials excel at certain applications where resistance to heat, high voltage or high frequencies is neces-



sary.²⁴⁷ However, these compound or wide-bandgap (WBG) wafers are more costly to produce, and although their market share is quickly growing for certain applications, it is still miniscule.

The market

The global **silicon wafer** market has been stable at around USD 11 billion for the past three years.²⁴⁸ But the market is also highly concentrated. With the successful acquisition²⁴⁹ of *Siltronic (Germany)* by *GlobalWafers (Taiwan)*, four companies will control more than 90% of the global market: *Shin-Etsu (Japan)*, *Sumco (Japan)*, *GlobalWafers (Taiwan)* and *SK Siltron (Korea)*.²⁵⁰

Silicon wafers are cut out of monocrystalline ingots made from polycrystalline silicon. The supplier market for this highly pure (99.999999999%)²⁵¹ polycrystalline silicone is similarly concentrated. *Wacker (Germany)*, *Hemlock (US)* and *Tokuyama (Japan)* control more than 80% of the market.

Compared to silicon, the global market for **SiC wafers** is significantly smaller, around USD 400 million, and less concentrated.²⁵² Important SiC wafer suppliers are *Cree (US)*, *Showa Denko (Japan)*, *Rohm (Japan)* and *GT Advanced Technologies (UK)*.²⁵³

Barriers to entry

Similar to chemicals and other semiconductor materials, key barriers to entry are the high purity and planeness requirements. The quality of the wafer has a direct impact on the yield rate of the fab. At the same time, 300mm silicon wafers account for only around 5% of a fab's operational costs. Thus, fabs are hesitant to switch to new wafer suppliers.²⁵⁴

The Chinese government's efforts to increase self-reliance

The 2014 Outline and the MiC 2025 roadmap targeted 300mm and 200mm wafers as a “*production line key material*.” In 2019, it was estimated that the state subsidized around 20% of the raw wafer price for purchases by Chinese firms.²⁵⁵ Raw wafer production is heavily emphasized in the current crop of subnational governments' IC development plans, perhaps reflecting anticipation of constraints on foreign-sourced supplies due to the worsening international political climate.

Competitive position of the Chinese industry



China's wafer production capacity remains relatively low by international standards. Many Chinese firms have developed technology for 300mm and 200mm wafers, although the quality and production still appear to significantly lag those of the global leaders.²⁵⁶

The 14th Five-Year Plan highlighted compound or “third-generation” wafer materials as a development priority, and in May 2021, they were likely discussed under the rubric of “post-Moore disruptive technologies” at a meeting of the ST&I SLG concerning implementation of the Five-Year Plan.²⁵⁷ Shanghai's 2021–2025 IC Development plan emphasizes development of 300mm wafer production and third-generation wafer materials (SiC and GaN), with ambitions for a “silicon carbide valley” concentrating SiC-related materials production.²⁵⁸ A National Innovation Centre for Third Generation Semiconductors was approved in early 2021 to be located in the Suzhou Industrial Park, a high-tech development zone close to Shanghai and several nationally leading institutes in Suzhou conducting semiconductor-related research.²⁵⁹

Likelihood of China catching up within 5 to 10 years

Although raw wafers could be viewed as a commodity in the semiconductor value chain, they are a foundational component in which quality and reliability are at a premium. Thus, Chinese producers are unlikely to be able to compete on price alone with international customers. As is often the case across the value chain, the dominant market share and technological advancement of existing leaders in this sector outside China mean that Chinese firms will likely remain restricted to lower-end products and domestic customers over the next 5 to 10 years in the case of silicon wafers.²⁶⁰

However, China's prospects in SiC/GaN look better. In 2016, an expert identified a concerted effort to develop an “integrated compound semiconductor value chain,” by leveraging China's huge market for relevant applications (lighting and power management electronics), the Big Fund's support and recruitment of foreign industry experts. This position was reflected in significant Chinese representation on SEMI's newly established Power and Compound Semiconductors Committee in 2015.²⁶¹ *Huawei's* leveraging of GaN-based power amplifiers for radio antennas in 5G market leadership is an early sign of what might be possible for Chinese firms in this field.²⁶²

Strategic dimensions



Competitiveness dimension

The **low revenue capture** combined with **moderate spillover benefits** and **substantial market-entry barriers** make silicon wafers an unattractive market to enter from an economic perspective. At the same time, high-quality wafers are a prerequisite for China's increased self-reliance in fabs. Moreover, the market is less concentrated than in other areas and has relatively high growth potential in compound semiconductors, making the wafer production market more attractive for China to enter. **Spillover benefits** are potentially higher for compound semiconductors, given the demand from China's wider manufacturing sector for relevant applications such as power semiconductors and radio frequency chips.

National security dimension

In theory, silicon wafers are a **substantial chokepoint** for Chinese fabs as they almost exclusively rely on non-Chinese wafer suppliers. However, this chokepoint has not been exploited by the U.S. government because there are no dominant U.S. wafer suppliers, or U.S. firms dominant in the upstream value chain for foreign wafer suppliers. This explains why (compared to other critical inputs, such as chemicals, SME or EDA) wafers have not played a key role in the US–China technology rivalry. However, silicon wafers have been subject to U.S. export restrictions in the past.²⁶³

Resilience dimension

In the case of a supply shortage, there would be **substantial spillover damage**. Without wafers, fabs cannot manufacture chips. However, the silicon and compound wafer markets are less **concentrated** than other inputs and process steps, and fabs typically source from several suppliers. The trend toward increased wafer production capacity in China may also increase the resilience of the global supply chain: Raw wafer production does not imply espionage risk, and much Chinese wafer production will likely (due to its relatively lower quality) service domestic demand, making more capacity available in wafer fabs outside mainland China.

Assembly, Test and Packaging: The Back-End (process step)

Assembly, test and packaging (ATP) is the last step in the semiconductor manufacturing process after wafer fabrication. The finished silicon wafer must be sliced, and the individual chips must be tested and packaged. Just like front-end fabs, back-end fabs rely on equipment and chemicals suppliers. The back-end processes are significantly less complex, the equipment less expensive and the requirements for the purity of chemicals lower. IDMs and foundries either have their own back-end fabs or rely on outsourced semiconductor assembly and test (OSAT) companies that specialize in these process steps. The back-end processes are labor-intensive and have lower profit margins.²⁶⁴ OSAT companies maintain very close relationships with

IP and EDA vendors as well as fabs. New packaging technologies become increasingly important to ensure cost-effective and energy-efficient chips. In this regard, heterogeneous integration is an innovation with high potential.²⁶⁵ Advanced packaging also increases the complexity of back-end processes and leads to necessarily closer collaboration between front-end and back-end as well as chip design.²⁶⁶

The Market

Market consolidation, as a typical feature of the semiconductor value chain, applies to the OSAT market as well. The 20 largest companies held 92% of the market in 2019 and are geographically concentrated. Today, 9 of the 10 largest OSAT providers are located in mainland **China**, **Taiwan** and **Singapore**.²⁶⁷ **China** and **Taiwan** alone make up more than 60% of the global OSAT capacity. **North America** accounts for only 3% of the global OSAT capacity.²⁶⁸

The global packaging market had a value of USD 43 billion in 2019.²⁶⁹ The largest OSAT company by revenue is *ASE Group (Taiwan)* with USD 8.5 billion revenue in 2019.²⁷⁰ Second in line is the only large OSAT company headquartered in the **United States**: *Amkor Technologies* (USD 4.31 billion revenue),²⁷¹ which fabricates in **Korea**, **Taiwan**, **China** and **Malaysia**.^{272, 273} The OSAT market in **Singapore** and **Malaysia** has lost market share over the last 10 years, but **Chinese** companies, such as *JCET* (third largest global OSAT company²⁷⁴), increased their share significantly to 19%, compared to *ASE Group* with 26% in 2019.²⁷⁵

Barriers to Entry

Although the market consolidated over the past 15 years, it is less concentrated than cutting-edge wafer fabrication, and there are fewer barriers to entry in comparison. Similar to fabrication, OSAT companies rely on equipment suppliers and chemicals. But market entry for OSAT companies requires less capital, due to cheaper and less complex equipment and chemicals. Because IDMs and foundries are OSAT companies' customers, establishing these relationships is a market-entry barrier.²⁷⁶ However, the market's standout feature is labor intensity, and high labor costs are inevitable. For that reason, back-end processes have been primarily outsourced, resulting in their current geographic concentration.

One key to success in ATP is close cooperation with EDA vendors and IP suppliers as well as foundries. As chips become more complex, and advanced packaging be-



comes more important, OSAT companies need to be linked to the ecosystem with material and equipment suppliers as well as access to R&D.²⁷⁷

The Chinese government's efforts to increase self-reliance

China instituted multiple packaging-related R&D projects under the 02 Special Project, and the 2014 Outline, MiC 2025 roadmap and 2016 National Informatization Plan all emphasized developing various packaging techniques. By 2017, authorities claimed that China's "*packaging enterprises had moved from low-end to high-end, and three-dimensional high-density integration technology had reached internationally advanced levels.*"²⁷⁸ Combined with the market's structural features, this advancement has allowed Chinese firms to capture their largest market share across the global value chain in this process step.

The 2014 Outline also advocated consolidation of the domestic packaging and test sector through corporate mergers. With this approach, China's three leading firms in this sector more than tripled their share of the global top 10 companies' revenues over 2011–2017, moving on to international acquisitions.²⁷⁹ In 2015, the Big Fund helped underwrite a USD 780 million buyout by state-backed *JCET* of the world's then-fourth largest packaging and testing firm in Singapore. In 2016, the Big Fund supported the creation of a joint venture between *Tongfu* and U.S. industry leader *AMD*'s subsidiaries in China and Malaysia, giving *Tongfu* access to more advanced packaging technologies.²⁸⁰ However, this outbound M&A has met obstacles in the packaging and test sector, as elsewhere. For example, *Tsinghua Unigroup*'s attempted simultaneous acquisitions in 2015 of Taiwan's second, third and fourth largest chip assembly firms were blocked by Taiwanese authorities for security reasons.²⁸¹

Chinese authorities are also watching global trends in modular manufacturing and other cutting-edge developments in packaging. The city of Zhuhai's 2020–2025 IC Development Plan aims to build a RMB 10 billion manufacturing cluster around compound semiconductors, modular manufacturing and packaging and test.²⁸² In 2019, the Big Fund's managing entity stated that its Phase II investments would seek to promote integration of ATP with equipment and fabrication in a "virtual IDM model".²⁸³ Multiple subnational governments are providing subsidies for ATP-related items, including with specific reference to applications and materials such as power semiconductors or compound semiconductors (silicon carbide and gallium nitride) that were prioritized in the 14th Five-Year Plan.

Competitive position of the Chinese industry

Between 2012 and 2019, China's share of the global ATP sector increased from 5% to 20%, and three of the top six firms by sales are now Chinese, compared to one six years ago.²⁸⁴ More than 20% of the world's assembly and test facilities are now located in China.²⁸⁵ However, this rapid growth was driven heavily by foreign M&A activity, which for political reasons is unlikely to continue. Political concerns about Chinese firms may also remove another component of domestic firms' success in this segment of the value chain: joint ventures with foreign industry leaders, which are unusual as multinationals in China's semiconductor sector are typically present as branch offices or wholly foreign-owned enterprises.²⁸⁶

Worsening political relations with the US may also impact business operations of Chinese ATP firms. Even if these firms can securely source equipment from non-US suppliers, the firms are exposed on the demand side due to U.S. dominance in other value chain segments. *Tongfu*, for example, makes around half its revenue from U.S. customers.²⁸⁷ This risk is aggravated by relatively slim operating margins.²⁸⁸

The innovation activity of Chinese firms in this sector also appears lower compared to chip design or manufacturing, as measured by patent filings in mainland China. However, these filings also reflect a high degree of indigenization. Domestic rights-holders account for 91% of these ATP-related patents and hold more patents in each category than foreign rights-holders.²⁸⁹

Likelihood of China catching up within 5 to 10 years

As a downstream production step, ATP in China will benefit from growth in the Chinese chip design and fab sectors. Domestic firms are now competitive in this field, and ATP's role in the value chain means that foreign firms have little incentive to avoid Chinese providers, barring interference by foreign export controls. Combined with Chinese authorities' quest for "leapfrog" solutions, these factors are likely to focus government support on pushing technological developments in the domestic ATP sector. Some Chinese experts advocate for advanced packaging as the best way to drive forward China's entire semiconductor sector, if access to cutting-edge lithography equipment is cut off.²⁹⁰

However, unless Chinese firms can stay abreast of advances in packaging technology, the firms may suffer from a shift in comparative advantage to firms higher up in the value chain, as this process step becomes less labor-intensive and increasingly driven by capital and accumulated intellectual property. High-end advanced packaging remains dominated by non-mainland Chinese firms. *TSMC* leads in this segment, and *Intel* (US) is also investing heavily.²⁹¹ Security concerns about packaging will exert pressure to avoid outsourcing ATP to China, potentially reducing opportu-



nities for Chinese ATP firms to drive their own technological development by working with global leaders in design and fabrication.

Strategic dimensions

Competitiveness dimension

Historically, ATP has had significantly lower value-add and profit margins than chip design or fabrication, making market dominance in ATP relatively less significant in **revenue** terms. As a labor-intensive downstream process step, ATP provides **low spillover benefits** within the semiconductor value chain. Because there are only **moderate barriers to entry**, this step is less geographically concentrated and consolidated at the firm level than some of the other production steps.

If ATP becomes more skill-intensive due to the increasing importance of advanced packaging and less labor-intensive due to higher automation, the value of market dominance in this production step from a national interest viewpoint is likely to increase.

National security dimension

ATP has strategic importance because of the **high espionage risk**.²⁹² Compromising a chip in a back-end fab is significantly easier than during design or wafer fabrication.²⁹³ This poses a conflict of interest between governments and industry. From a national security perspective, the back-end fab should be a trusted entity ideally within the same jurisdiction. From a business perspective, the back-end process has been outsourced to Taiwan and China due to low profit margins, low value-add and high labor costs.²⁹⁴ The risk of espionage might lead the U.S. government and others to pressure or compel their firms not to outsource the ATP process to China.

However, efforts to mitigate such risks will face commercial obstacles until more advanced techniques make the economics of re-shoring OSAT to the US and its advanced-economy allies more feasible. The likely alternative locations to China (barring Taiwan) are Southeast Asian countries, which are increasingly closely integrated economically with China. Thus, shifting ATP processes to these countries may not adequately mitigate security concerns relating to China.

Resilience dimension

Compared to EDA or cutting-edge fabrication, the global ATP sector is not excessively concentrated at the firm level. However, ATP is geographically concentrated in China and Taiwan, and a significant disruption in both jurisdictions at once (for instance, in the event of a military conflict across the Taiwan Strait) would have serious ramifications for the global value chain.²⁹⁵



Generally speaking, disruptions in the back-end cause limited spillover damage in the semiconductor value chain itself, but there is potential for **substantial spillover damage** in the broader economy. This can be seen in the current chip shortages worldwide that are partly due to disruptions in the ATP sector.

The **concentration** of ATP processes in China, Taiwan and Southeast Asia exposes front-end manufacturers to business continuity risks.²⁹⁶ However, **replication of this production step** elsewhere is relatively easily achieved, given the relatively low barriers to entry and the competitive position of U.S. firms in pushing forward packaging developments. Leadership in advanced packaging techniques will also reduce the opportunity costs of diversifying ATP processes away from their current locations of concentration.

4. Conclusion and implications for Europe

China has a significantly stronger position across the entire semiconductor value chain today compared to 10 years ago. Despite persistent inefficiencies and weaknesses in the Chinese ecosystem for semiconductor R&D and production, China should be expected to continue strengthening its national position in the global value chain during this decade. Our analysis of the different production steps has illustrated various reasons for which China will continue to invest in its domestic semiconductor ecosystem, with different strategic implications associated with each production step. Our three strategic dimensions and their criteria provide a framework for assessing the implications of a Chinese semiconductor ecosystem that is slowly but steadily increasing its capabilities across the board.

From a European perspective, the main takeaways can be summarized as follows.

Competitiveness dimension: The production steps in which China's efforts are mainly driven by economic incentives are **chip design, IP, trailing-edge wafer fabrication, chemicals** and **ATP**. In some of these production steps, China's domestic industry is already significantly stronger than Europe's: China's global market shares in chip design, trailing-edge wafer capacity and ATP are multiple times larger than those of Europe.²⁹⁷ In these production steps, Europe risks not only falling behind still further but also increasingly relying on Chinese technology providers. In the case of chemicals, European suppliers already enjoy a strong market position but might face increasing competition from Chinese suppliers in the future, especially for chemicals and materials needed in ATP and wafer fabrication at mature nodes. If the Chinese government continues to substantially invest in its domestic chemicals suppliers, a similar development could unfold as with the solar industry, in which Chinese suppliers rapidly displaced European ones in markets worldwide.²⁹⁸

National security dimension: Especially in **EDA** and **SME**, national security considerations trump all other strategic considerations for China. Both are effective chokepoints vis-à-vis China that the U.S. government will most likely continue to utilize. Europe has critical suppliers in both production steps (*ASML* for SME and *Mentor* for EDA due to the acquisition by *Siemens*). Thus, the U.S. government will most likely push for bilateral agreements to achieve more extensive restrictions on exports to China than are presently contained in multilateral agreements like *Wassenaar*. SME vendors, especially for lithography equipment, rely on various European component suppliers (such as *Zeiss* (DE) for lenses and *Trumpf* (DE) for lasers). Therefore, Chinese SME vendors are likely to try sourcing these components instead of the complete equipment, and increasingly as their capabilities generally improve. The question is whether Europe will align with the U.S. government's approach of expanding export restrictions via these chokepoints.



Resilience dimension: The process step with the highest geographic concentration is certainly **cutting-edge wafer fabrication**. Although the Chinese government is unlikely to succeed in bringing cutting-edge wafer fabrication to China within this decade, the same is most likely true for Europe.²⁹⁹ The U.S. is currently in the best position to increase the resilience of the global cutting-edge wafer fabrication supply chain through *Samsung's* and *TSMC's* investments in new US-based fabs within the next five years. However, the **ATP** supply chain, especially for future advanced packaging approaches, must also be geographically diversified. In this, success for Europe is much more likely, not least because of significantly lower barriers to entry.

The European Union (EU) has introduced a range of initiatives to promote the European semiconductor industry. The Important Project of Common European Interest (IPCEI) on Microelectronics 2 allows member states to subsidize the construction of fabs and first industrial deployments.³⁰⁰ A joint declaration among 22 member states in December 2020 declared they would strategically invest in the EU's semiconductor ecosystem.³⁰¹ Semiconductors also play a central role in the EU's 2030 Digital Compass³⁰² and its New Industrial Strategy.³⁰³

However, Europe increasingly needs to account for **U.S. pressure** for coordinated measures regarding China's semiconductor industry. Two days before China passed its Counter-Sanctions Law, the U.S. Congress passed the USD 250 billion US Innovation and Competition Act, directed at equipping the US for long-term science and technology competition with China.³⁰⁴ The act provides for USD 52 billion in subsidies to promote the U.S. semiconductor industry.³⁰⁵ U.S. President Biden declared in his press release concerning the act's passage, "We are in a competition to win the 21st century, and the starting gun has gone off."³⁰⁶ Competition with China on a global scale, particularly in strategic technologies including semiconductors, appears to be a primary concern of the Biden administration that will shape the future of the US–Europe relationship across many areas.³⁰⁷

Semiconductors were reportedly discussed by European and U.S. policymakers in June 2021 at the G7-Plus summit. This forum was also attended by South Korea and Japan, two U.S. security allies that occupy key roles in the semiconductor value chain. The Leaders' Communique from this summit declared that the G7 nations will "consider mechanisms and share best practices to address risks to the resilience of the critical global supply chains, in areas such as critical minerals and semiconductors, reflecting on models used elsewhere such as stress-testing."³⁰⁸

Straight after the G7-Plus summit, the EU and the U.S. agreed on a Trade and Technology Council to coordinate "to coordinate approaches to key global trade, economic, and technology issues", although reporting suggests that European officials have qualified expectations for this process.³⁰⁹ The NATO summit in June 2021 set a stron-



ger tone for potential U.S.–European cooperation on strategic technology matters involving China, declaring that “China's growing influence and international policies can present challenges that we need to address together as an Alliance.”³¹⁰

In crafting the best policy mix to address all these issues, consideration must be given to **China's increasing readiness to punish other countries and their firms** for real or perceived measures that discriminate against Chinese entities. In June 2021, China adopted a Counter-Sanctions Law that empowers Chinese authorities to claim damages or seize assets from entities deemed to be aiding enforcement of measures by foreign governments that are deemed discriminatory to Chinese interests.³¹¹ This potentially includes export and investment controls concerning semiconductors. China has also adopted or will soon adopt a range of other laws, including laws covering export controls, data governance and foreign investment, that provide for such retaliatory measures.³¹² As the president of the European Chamber of Commerce in China recently put it, in this environment European firms “*increasingly feel that they will be used as sacrificial pawns in a game of political chess.*”³¹³

However, it is important that European decisionmakers do not interpret this situation as a Chinese quest for technological autarky, at least within the next 10 years. China's leaders have made clear their intention for China's economy, including the semiconductor sector, to remain integrated with the outside world. A Chinese technical expert stated recently, “*The development of ICs has to be globalized ... There's no future for unilateralism pushed by certain countries.*”³¹⁴ The challenge from the European viewpoint is that Chinese authorities will try to shape such globalization to operate on terms that are increasingly beneficial for China, and to move Chinese firms into a position of international leadership that will inevitably challenge some European interests.

European leaders need to find the optimal balance on semiconductor policy across this range of issues **that serves European interests**, rather than being led by pressure from other national actors, force of circumstance or excessive focus on one strategic dimension of national interest at the expense of others. This report has provided a framework for assessing these issues in terms of China's position in the global value chain, and the impacts this position has on other actors' national interests. A second report, to be published by the end of 2021, will dive deeper into the implications from a European viewpoint in the global context.



Annex 1: Technical Terms Glossary

AI	Artificial Intelligence
ATP	assembly, test & packaging
ArF	argon fluoride
Back-end	assembly, test & packaging (ATP)
Compound Semiconductors	Semiconductors composed of two or more elements
CPU	Central Processing Unit
CSIA	China Semiconductor Industry Association
DRAM	Dynamic Random Access Memory
DUV	deep-ultraviolet lithography (EUV predecessor)
EDA	electronic design automation
ESL	Electronic System Level
EUVL	extreme-ultraviolet lithography
EV	electric vehicles
Fab	fabrication plant
Foundry	company that does contract chip manufacturing
FPGA	field programmable gate array
Front-end	Wafer fabrication (process steps before ATP)
GaAs	gallium arsenide
GaN	gallium nitride
ICT	Information and communications technology
IDM	Integrated Device Manufacturer
Imec	Interuniversity Microelectronics Centre
IC	integrated circuit (also called "chips")



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IT	Information technology
IoT	Internet of Things
IP	Intellectual Property
ISA	instruction set architectures
NAND	non-volatile flash memory
OSAT	outsourced semiconductor assembly and test
PDK	process design kits
RF	radio frequency
S&T	Science & Technology
S&TI	Science, Technology & Innovation
SME	Semiconductor manufacturing equipment
SoC	System on Chip
Si	silicon
SIA	US Semiconductor Industry Association
SiC	silicon carbide
WBG	wide-bandgap



Annex 2: Chinese Terms and Acronyms Glossary

Big Fund	National Integrated Circuit Industry Investment Fund (国家集成电路产业投资基金)
Government Guidance Fund	Government Guidance Fund (国家集成电路产业投资基金)
IC Industry Dev LSG	Leading Small Group for Development of the National Integrated Circuit Industry (国家集成电路产业发展领导小组)
LSG	Leading Small Group (领导小组)
Mic 2025 Roadmap	"Made in China 2025" Roadmap of Key Technologies (《中国制造2025》重点领域技术路线图)
MiC 2025	Made in China 2025 (中国制造2025) industrial upgrading strategy
MIIT	Ministry of Industry and Information Technology (工信部/工业和信息化部)
MOF	Ministry of Finance (财政部)
MOST	Ministry of Science and Technology (科技部)
NDRC	National Development and Reform Commission (发改委/国家发展和改革委员会)
NMLTP	National Medium & Long Term Plan for Science and Technology (2006–2020) (国家中长期科学和技术发展规划纲要2006–2020) (new iteration for the period 2021-2035 forthcoming)
SOE	State Owned Enterprises (国有企业)
State Council	State Council (国务院)
ST&I LSG	Leading Small Group for Reform of the National Science and Technology System and Building an Innovation System (国家科技体制改革和创新体系建设领导小组)
Third Generation Semiconductor	Compound semiconductors (第三代半导体)
02 Special Project	02 Special Project for Very Large Scale Integrated Circuit Manufacturing Equipment and Complete Processes (极大规模集成电路制造装备及成套工艺02专项, under NMLTP (2006–2020))
13th FYP	13th Five Year Plan for Economic and Social Development (2016–2020) (十三五规划/中华人民共和国国民经济和社会发展第十三个五年规划纲要)



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14th FYP

14th Five Year Plan for Economic and Social Development (2021–2025) and 2035 Long-Term Vision (十四五规划/中华人民共和国国民经济和社会发展第十四个五年规划和2035年远景目标纲要, March 2021)

14th FYP S&TI

14th Five Year Plan for Science & Technology Innovation (forthcoming) (“十四五”国家科技创新规划)

2014 Outline

National Integrated Circuit Industry Development Outline (国家集成电路产业发展推进纲要 (2014))



Annex 3: Chinese official policy documents and selected other sources

(By category, in descending chronological order)

1. National-level policies

Title	Issuing Authority
National Medium & Long Term Plan for Science and Technology (2006-2020) 国家中长期科学和技术发展规划纲要2006-2020	State Council (2005)
National Integrated Circuit Industry Development Outline 2014 ("2014 Outline") 国家集成电路产业发展推进纲要 (2014)	State Council (2014)
Made in China 2025 Roadmap of Key Technologies ("MiC Roadmap") 《中国制造2025》重点领域技术路线图	Chinese Academy of Engineering (2015)
13th Five-Year Plan for the Development of National Strategic Emerging Industries “十三五”国家战略性新兴产业发展规划	State Council (2016)
13th Five-Year National Informatization Plan “十三五”国家信息化规划	State Council (2016)
Guiding Catalogue for Strategic Emerging Industries Key Products and Services 战略性新兴产业重点产品和服务指导目录	NDRC (2017)
Catalogue of Encouraged Foreign Investment (2019) 鼓励外商投资产业目录 (2019年版)	NDRC (2019)
Implementation Opinions on Promoting the Improvement of the Quality of Manufacturing Products and Services 工业和信息化部关于促进制造业产品和服务质量提升的实施意见	MIIT (2019)
Outline for the Integrated Development of the Yangtze River Delta 长江三角洲区域一体化发展规划纲要	CCP Central Committee, State Council (2019)
Some Policies to Promote the High-Quality Development of the Integrated Circuit and Software Industry in the New Era 新时期促进集成电路产业和软件产业高质量发展的若干政策	State Council (2020)



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Title	Issuing Authority
Announcement on the Enterprise Income Tax Policy for Promoting the High-quality Development of the Integrated Circuit and the Software Industry 关于促进集成电路产业和软件产业高质量发展企业所得税政策的公告	MOF, MIIT, NDRC (2020)
Circular on Import Tax Policies for Supporting the Development of the Integrated Circuit and Software Industry 关于支持集成电路产业和软件产业发展进口税收政策的通知	MOF, General Administration of Customs, State Taxation Administration (2021)
14th Five Year Plan for Economic and Social Development (2021-2025) and 2035 Long-Term Vision 十四五规划/中华人民共和国国民经济和社会发展第十四个五年规划和2035年远景目标纲要	State Council (2021)
14th Five Year Plan for Science & Technology Innovation (forthcoming) “十四五”国家科技创新规划	State Council (2021)
National Medium & Long Term Plan for Science and Technology (2021-2035) (forthcoming) 国家中长期科学和技术发展规划纲要2021-2035	State Council (2021)

2. Province-level policies

Title	Issuing Authority/Date
Fujian Provincial People's Government Opinions on Accelerating the Development of the Integrated Circuit Design Industry 福建省人民政府加快发展集成电路设计业的意见	Office of Fujian Provincial People's Government (2007)
Shanghai Municipal People's Government Policies to Further Encourage the Development of the Software and Integrated Circuit Industries 上海市人民政府关于本市进一步鼓励软件产业和集成电路产业发展的若干政策	Shanghai Municipal People's Government (2012)
Anhui Provincial People's Government Opinions on Accelerating the Development of the Integrated Circuit Industry 安徽省人民政府办公厅关于加快集成电路产业发展的意见	Office of Anhui Provincial People's Government (2014)



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Titel	Issuing Authority/Date
Shandong Provincial People's Government Opinions on Accelerating the Development of Integrated Circuit Industry by Implementing No.4 Document (2014) of the State Council 山东省人民政府关于贯彻国发(2014)4号文件加快集成电路产业发展的意见	Shandong Provincial People's Government (2014)
Hubei Province Action Plan for the Development of the Integrated Circuit Industry 湖北省集成电路产业发展行动方案	Hubei Provincial People's Government (2014)
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Titel	Issuing Authority/Date
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<p>Tianjin Binhai New District Opinions on Accelerating the Development of the Integrated Circuit Design Industry</p> <p>天津市滨海新区加快发展集成电路设计产业的意见</p>	Tianjin Binhai New District People's Government (2014)



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Titel	Issuing Authority/Date
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Nanjing Municipal Government's Opinions on Advancing the Development of the Integrated Circuit Industry 南京市政府关于加快推进集成电路产业发展的意见	Nanjing Municipal People's Government (2016)
Wuxi Municipality Policy Opinions on Accelerating the Development of the Integrated Circuit Industry 无锡市加快集成电路产业发展的政策意见	Wuxi Municipal People's Government (2016)
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Hangzhou Municipal Integrated Circuit Development Plan 杭州市集成电路产业发展规划	Office of Hangzhou Municipal People's Government (2017)
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Titel	Issuing Authority/Date
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Some Implementation Policies to Promote the Development of the Integrated Circuit Industry in Zhuhai 关于促进珠海市集成电路产业发展的若干政策措施	Office of Zhuhai Municipal People's Government (2020)
Some Policies on Accelerating the High-Quality Development of the Integrated Circuit Industry in Wuhan 武汉市加快集成电路产业高质量发展若干政策	Wuhan Municipal People's Government (2020)
Implementation Plan to Advance an Economic Development Zone to Innovate and Build New Heights in Reform and Opening Up 南京市推进经济开发区创新提升打造改革开放新高地实施方案	Nanjing Municipal People's Government (2021)
Special Plan for the Integrated Circuit Industry in the Lingang New Area of China (Shanghai) Pilot Free Trade Zone (2021–2025) 中国(上海)自由贸易试验区临港新片区集成电路产业专项规划 (2021–2025)	China (Shanghai) Lingang New Pilot Free Trade Zone (2021)
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